



The bridge to possible

Data sheet
Cisco public

Cisco Silicon One Q100 and Q100L Processors

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The silicon industry has always been plagued with the trichotomy of switching silicon, routing line card silicon, and routing fabric silicon. Using these three basic building blocks, silicon and system vendors created unique architectures tuned for individual markets and industries. Consequentially, forcing customers to consume and manage these disjointed and dissimilar products caused an explosion in complexity, CapEx, and OpEx for the industry.

The Cisco Silicon One™ architecture ushers in a new era of networking, enabling one silicon architecture to address a broad market space, while simultaneously providing best-of-breed individual devices.

At 10.8 Tbps, the Cisco Silicon One Q100 is the first member of the Cisco Silicon One family. It provides high bandwidth, high performance, exceptional flexibility and optimal power efficiency.

Product overview

The Cisco Silicon One Q100 Processor can be configured using its P4 run-to-completion network processor into one of the following modes:

- Q100
 - 10.8-Tbps, full-duplex, stand-alone routing processor with deep buffers
 - 5.4-Tbps, full-duplex, line card routing processor with deep buffers
- Q100L
 - 10.8-Tbps, full-duplex fabric element

Cisco Silicon One Q100 and Q100L processors can be used to build a wide range of products covering fixed form factor routers, modular chassis routers and multipetabit disaggregated routers.

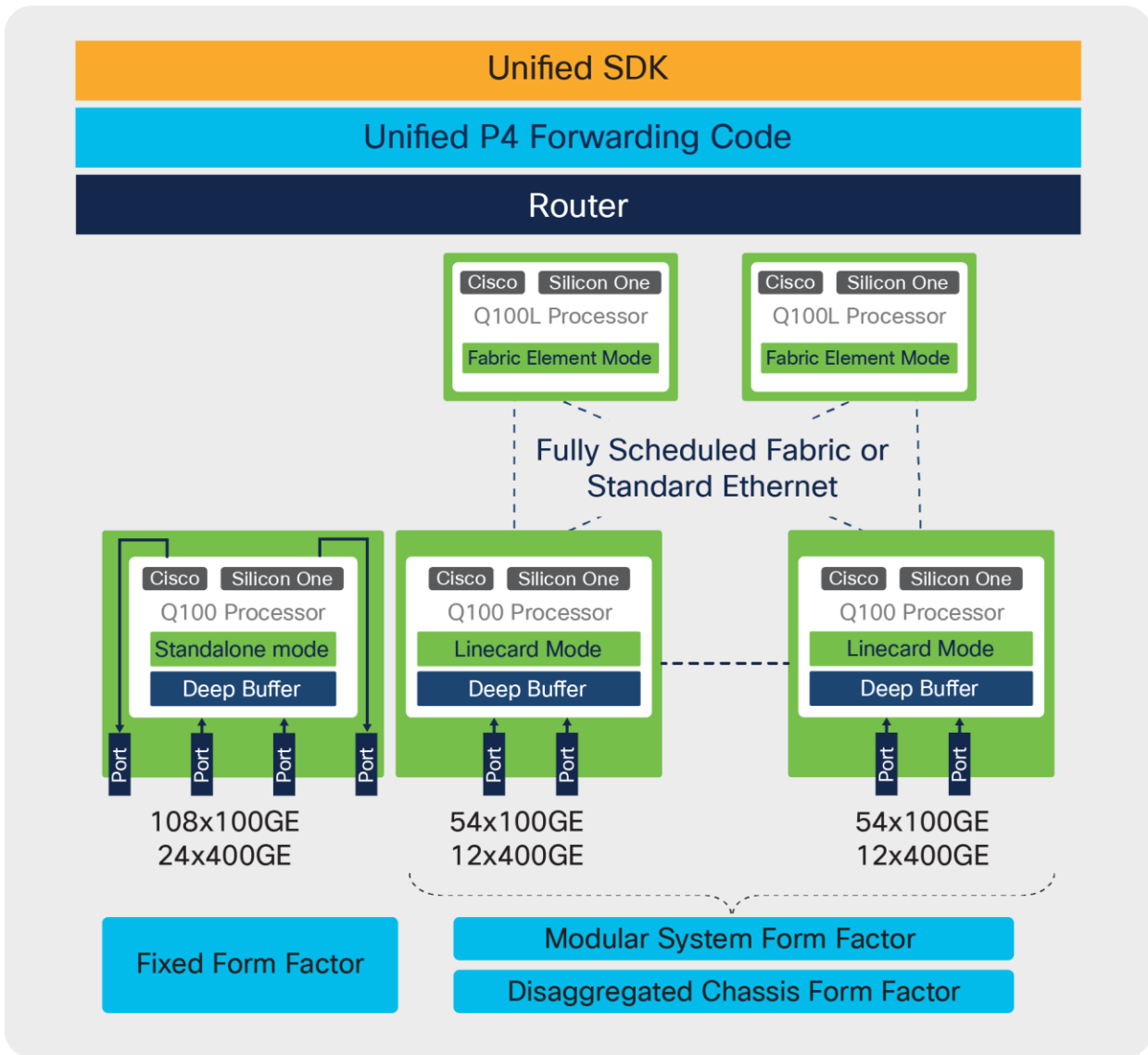


Figure 1.
Form factors

Features and benefits

Table 1. Architectural characteristics and benefits

Feature	Benefit
Unified architecture across multiple markets	Greatly simplifies customer network infrastructure deployments
Unified SDK across market segments and applications	Provides a consistent point of integration for all applications across the entire network infrastructure
High-bandwidth routing and fabric silicon	10-Tbps+ routing and fabric silicon
High-performance routing silicon	Achieve line rate at small packet sizes

Feature	Benefit
Power efficient routing silicon	The power efficiency of 16nm and the Cisco Silicon One architecture
Large and fully unified packet buffer	Fully shared on-die buffer with optional large, external packet buffer
Highly scalable routing features	Ideally targeted to address core, peering and DCI applications
Run-to-completion network processor	Provides industry-leading flexibility without compromising performance or power efficiency
P4 Programmable	Leverages an open source programming language to enable customers to define their own features

Flexibility, Performance, and Scale for Next-Generation Service Provider and Web-Scale Networks

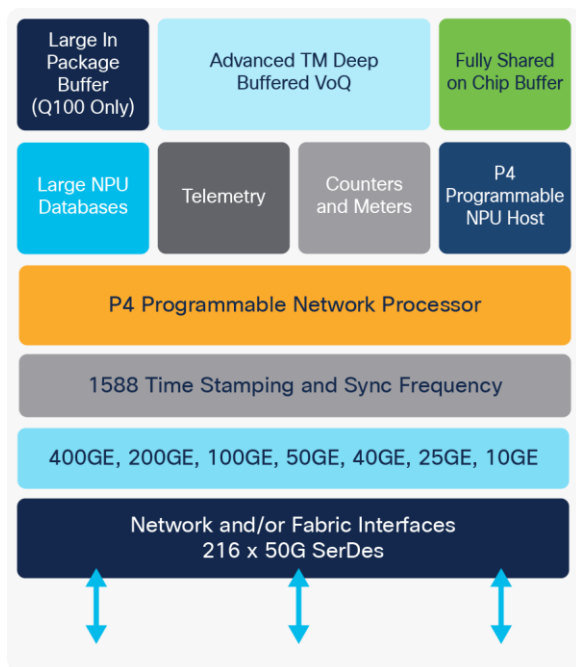


Figure 2.
Block Diagram

Features

- 216 56G SerDes, each can be configured independently to operate in 10G/25G/50G using NRZ or PAM4 modulation
- Flexible port configuration supporting 10/25/40/50/100/200/400 Gbps
- Large, fully shared, on-die packet buffer
- Large, in-package packet buffer (Q100 only)
- 1588v2 and SyncE support with nanosecond-level accuracy
- On-chip, high-performance, P4-programmable host NPU for high-bandwidth offline packet processing (for example, OAM processing, MAC learning)
- Multiple embedded processors for CPU offloading

Traffic management

- Large pool of configurable queues, supporting DiffServ and hierarchical QoS
- Support for system-level, end-to-end QoS and scheduling for both unicast and multicast traffic
- Seamless extension of on-die buffer to external packet buffer
- Support for ingress and egress traffic mirroring
- Support for link-level (IEEE802.3x), PFC priority-level (802.1Qbb) flow control, and ECN marking
- Support of port extenders

Network Processor

- Run-to-completion P4 programmable network processor
- Line rate at very small packets even with complex packet processing
- Large and shared fungible tables
- Support for complex packet processing features without impacting data rate
- Support for simple packet processing features with optimized power and latency

Load balancing

- Flow load balancing using ECMP or LAG
- Dynamic flowlet load balancing with ability to detect and handle elephant flows
- Packet-by-packet load balancing, creating an optimal, flow-independent, end-to-end scheduled and lossless fabric

Instrumentation and telemetry

- Programmable meters used for traffic policing and coloring
- Programmable counters used for flow statistics and OAM loss measurements
- Programmable counters used for port utilization, microburst detection, delay measurements, flow tracking, elephant flow detection and congestion tracking
- Traffic mirroring - (ER)SPAN on drop
- Support for sFlow and NetFlow

SDK

- APIs provided in both C++ and Python
- Configurability via high-level networking objects
- Distribution-independent Linux packaging
- Robust simulation environment enables rapid feature development
- CPU packet I/O through native Linux network interfaces

P4 Programmability

- Application development is handled by a P4-based IDE programming environment
- At compilation, the P4 application generates low-level register/memory access APIs and higher-level SDK Application APIs
- Provides application support for a wide range of datacenter, service provider and enterprise protocols
- Modifications to the provided application can be easily accomplished using the provided P4 development environment
- Ability to develop the SDK and applications running over the SDK over a simulated Cisco Silicon One device

Cisco P4 application

Due to Silicon One's extensible P4 programming toolkit, we are always adding features to address new markets and new customer requirements; however, a sample of the features that are currently available with the P4 code is provided below:

<ul style="list-style-type: none">• IPv4/v6 Routing<ul style="list-style-type: none">◦ OSPF◦ IS-IS◦ BGP• MPLS Forwarding<ul style="list-style-type: none">◦ LDP, LDPoTE◦ RSVP-TE◦ SR-MPLS◦ SR-TE◦ L3VPN, 6PE, 6VPE◦ BGP LU◦ VPWS/EoMPLS◦ VPLS• Ethernet Switching<ul style="list-style-type: none">◦ 802.1d, 802.1p, 802.1q, 802.1ad• IP Tunneling<ul style="list-style-type: none">◦ IPinIP◦ GRE◦ VXLAN• Integrated Routing and Bridging (IRB)• HSRP/VRRP• Policy-Based Routing• Security and QoS ACLs	<ul style="list-style-type: none">• ECMP and LAG (802.3ad)• Multicast<ul style="list-style-type: none">◦ PIM-SM/SSM◦ IGMP◦ MLDP◦ MVPN• NAT/PAT• Protection (Link/Node/Path and TI-LFA)• QoS Classification and Marking• Congestion Management• Telemetry<ul style="list-style-type: none">◦ NetFlow, sFlow◦ (ER)SPAN◦ Packet Mirroring with Appended Metadata◦ Lawful Intercept• DDoS Mitigation<ul style="list-style-type: none">◦ Control-Plane Policing◦ BGP Flowspec• Control-Plane Policing• Timing and Frequency Synchronization<ul style="list-style-type: none">◦ SyncE◦ 1588
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Cisco environmental sustainability

Information about Cisco’s environmental sustainability policies and initiatives for our products, solutions, operations, and extended operations or supply chain is provided in the “Environment Sustainability” section of Cisco’s [Corporate Social Responsibility](#) (CSR) Report.

Reference links to information about key environmental sustainability topics (mentioned in the “Environment Sustainability” section of the CSR Report) are provided in the following table:

Sustainability topic	Reference
Information on product material content laws and regulations	Materials
Information on electronic waste laws and regulations, including products, batteries, and packaging	WEEE compliance

Cisco makes the packaging data available for informational purposes only. It may not reflect the most current legal developments, and Cisco does not represent, warrant, or guarantee that it is complete, accurate, or up to date. This information is subject to change without notice.

Product sustainability

Information about Cisco’s environmental, social and governance (ESG) initiatives and performance is provided in Cisco’s CSR and sustainability [reporting](#).

Table 2. Cisco Environmental Sustainability information

Sustainability Topic		Reference
General	Information on product-material-content laws and regulations	Materials
	Information on electronic waste laws and regulations, including our products, batteries and packaging	WEEE Compliance
	Information on product takeback and reuse program	Cisco Takeback and Reuse Program
	Sustainability Inquiries	Contact: csr_inquiries@cisco.com

For more information

[Learn more](#) about the Cisco Silicon One

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Cisco Systems, Inc.
San Jose, CA

Asia Pacific Headquarters
Cisco Systems (USA) Pte. Ltd.
Singapore

Europe Headquarters
Cisco Systems International BV Amsterdam,
The Netherlands

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