White paper
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An Introduction to the Cisco Catalyst 8500L Edge Platform

Contents

This document provides a high-level overview of the Cisco Catalyst 8500L Edge Platform. It introduces the platform and compares it with the rest of the Catalyst 8500 Series.

Introducing the Cisco Catalyst 8500L Edge Platform

The Cisco® Catalyst® 8500L Edge Platform rounds out the Catalyst 8500 Series Edge Platform portfolio. While the rest of the 8500 Series fills the 100- to 200-Gbps forwarding profile, the 8500L platforms brings that same feature set to the 20-Gbps network position. This functional consistency is a tremendous advantage. Network architects and designers will be interested to learn what the 8500L adds to the Cisco ASR 1001-X platform as well as what it brings in consistency with the Catalyst 8500 platforms.

Cisco launched the all-new Cisco Catalyst 8500 Series Edge Platforms in late 2020. These platforms are next-generation successors to the Cisco ASR 1000 Series Aggregation Services Routers. The ASR 1000 Series platforms have delivered cutting-edge services combined with performance and encryption since their release in 2008. As Cisco moves forward in the edge and aggregation space, the Catalyst 8500 Series Edge Platforms are highly capable and purpose-built to address traditional WAN, emerging SD-WAN, and colocation use cases, continuing the success of the ASR 1000 Series.

In addition to the Cisco QuantumFlow Processor™ based C8500-12X4QC and C8500-12X platforms, there is the C8500L-8S4X platform. The C8500L-8S4X platform shares almost all of the features and behavioral characteristics of the two higher-end platforms. However, it uses a different data plane architecture to deliver that compatible feature set at a comfortable performance and price combination. The C8500L-8S4X and C8500-12X are the recommended migration paths for the ASR 1001-X and ASR1002-X, offering greater performance with similar price points.

First, however, the bar should be set for what all the Cisco Catalyst 8500 Series Edge Platforms deliver:

- Built-in processor(s) with dedicated cores for:
  - Data forwarding
  - Cryptography
  - Control plane
  - Services plane
- Redundant AC or DC power supplies
- On/off switches on the power supplies (AC and DC)
- Replaceable fan assembly
- Flexible 10G/1G interfaces for varied network topologies across all models
- Flexible 100G/40G interfaces (C8500-12X4QC)
- Optional RFID hardware

The Catalyst 8500L platform hardware is set apart because of its use of a 12-core Intel® x86 chip for the entirety of the platform's functionality. Depending on a user-addressable software configuration, the cores on that chip are dedicated to different functionalities. The cores are distributed among control plane, data plane, cryptography, and an optional services plane. This allows maximum flexibility for network functionality as needs potentially change over time.

Connectivity

Figure 1.
C8500L-8S4X connections

The C8500L-8S4X platform offers a 1-rack-unit solution that addresses the aggregation and edge network role with up to 20 Gbps of performance. The platform does this while providing eight dedicated 1G interfaces (8S) and four flexible interfaces that can be configured as either 1G or 10G speed (4X). All interfaces are active and require no port licensing. The full throughput of the platform is available as well. However, crypto throughput, via IPsec, is licensed at various levels of throughput. WAN MACsec is available on all interfaces and is not rate limited.

Control plane architecture

The Catalyst 8500L platform has a built-in control plane to establish route processor functionalities. Two of the twelve cores are always dedicated for control plane functionality.

The control plane implementation is responsible for the following functions:

- Running the router control plane, including network control packets and connection setup
- Synchronizing the active and standby processes in dual Cisco IOS® redundancy operation
- Code storage, management, and upgrades
- Onboard failure logging (OBFL)
- Downloading operational code for interface control blocks and forwarding processor, QFP over Ethernet out-of-band channel (EOBC), which is used for communication between the control processors on the 8500 Series
- The Command-Line Interface (CLI), alarm, network management, logging, and statistics aggregation
- Punt path processing of packets is not supported by the Catalyst 8500 or 8500L embedded services processors
- A configuration repository for logging system statistics, records, events, errors, and dumps of the management interfaces of the platform, including the console serial port
- The MGMT Ethernet (ENET) management ports, CLI, status indicators, USB ports for secure key distribution, and a micro-USB console
- The field-replaceable fan tray, power supply module, online insertion and removal (OIR) events, etc.
- The chassis management, including activation and initialization of the other hardware in the chassis, image management and distribution, logging facilities, distribution of user configuration information, and alarm control
- The control signals for monitoring the health of power entry modules, shutting down the power, and driving alarm relays located on the power entry modules

Data plane architecture

Traditionally the data planes of Cisco's enterprise edge and aggregation platforms have been based on the Cisco QuantumFlow Processor Application-Specific Integrated Circuit (ASIC). This architecture continued into the Catalyst 8500 Series with the use of the third-generation Cisco QuantumFlow Processor. That ASIC enables those platforms to deliver 100 Gbps and higher performance. Not all network locations require that level of performance, however. There are numerous deployments that require the same level of feature flexibility but a lower level of throughput. This is where the C8500L-8S4X platform excels. It offers virtually an identical set of features to that of the Catalyst 8500 platforms but at a lower performance point and, perhaps more crucially, a lower price point. The feature variation is specifically related to limited use cases requiring classification of ingress packets prior to processing by the data plane cores.

The major component driving this lower price point is the use of an Intel architecture for the data plane instead of the dedicated Cisco QuantumFlow Processor. For several years now, the Cisco 4300 Series Integrated Services Routers (ISRs) have delivered a complete set of features in the Cisco IOS XE operating system based on an Intel x86 architecture for both the control plane and data plane. The 8500L-8S4X platform brings the same basic architecture to a new place in the network. Simply adding the aggregation and edge feature set to an x86-based architecture was not enough to efficiently address the entry point positioning. In order to get maximum performance from the architecture, a flow-based forwarding algorithm was designed specifically for the Catalyst 8500L. This flow-based forwarding mechanism is what sets the 8500L platform apart from all of the other Cisco IOS XE-based routing platforms.

The implementation of this new flow-based forwarding mechanism did not leave any features behind. The complete and rich set of network functions that was available on the ASR 1000 and Catalyst 8500 Series platforms is available on the 8500L platform as well. Feature and configuration compatibility are expected and delivered with the Catalyst 8500L.

Flow-based forwarding algorithm

In the existing Intel x86-based 4300 Series ISRs, packets are given to any available core for processing, independent of which network flow it is part of. This allows for a simpler design but also introduces some specific inefficiencies. Because packets for a given flow are processed by different cores, memory must be addressed by different cores. Under certain conditions this can tax various levels of processor memory caches, potentially introducing inefficiencies and causing delays. The C8500L-8S4X platform takes a different approach with the flow-based forwarding algorithm. Incoming traffic is hashed and distributed among the various cores that are dedicated to the data plane. This means that all the packets associated with a single flow will be processed by a single core. This streamlining and consistent processing enables robust and efficient processing of traffic. A given core is very likely to have cached information readily available in the very fast Layer 1/Layer 2 processor caches. Having very quick access to this information speeds up the data forwarding process and allows the platform to get maximum performance from the data plane cores.

To take maximum advantage of all the data plane cores, it is very important that there is a wide distribution of flows that will hash against all the data plane cores. With the Catalyst 8500L platform being positioned as an edge/aggregation platform, this is the exact profile of traffic to be expected. Often traffic at this location in the network is encapsulated inside various types of tunnels, including Generic Routing Encapsulation (GRE) and IPsec tunnels. The diversity of addressing that makes for an ideal distribution of traffic is found in the encapsulated addressing and not the outermost tunnel address. For this reason, the Catalyst 8500L platform will inspect inside the tunnel encapsulations to get the packet header information used to build the flow to the core hashing database. This works even for traffic that is being decrypted, as the decrypt operation happens first and then the traffic is distributed to a data plane core based on the newly decrypted encapsulated packet.

Traffic flows can be hashed on several parameters depending on the packet encapsulation. Different encapsulations can necessitate the use of different fields. Some of the fields used include:

- IPv4 (source and destination addresses)
- IPv6 (source and destination addresses)
- MPLS labels
- VLANs (single and dual tags)
- UDP ports (source and destination)
- TCP ports (source and destination)
- Inspection inside GRE, IPsec, and SD-WAN tunnels to use the encapsulated headers for maximum flow diversity

Services architecture

The Cisco IOS XE operating system offers the ability to host applications on the platform very much like other hypervisor systems. Since there are an ample number of cores on the x86 System-on-Chip (SoC) used as the CPU for the Catalyst 8500L platform, there is flexibility in how those cores can be assigned. The default distribution of those cores is two each for control plane, queuing, and crypto, with the remaining six given to the data plane. This configuration maximizes the throughput for the platform. However, if hosted services are required on the platform, a software configuration followed by a reboot would redistribute those cores. In services mode the cores are redistributed. The services configuration has two cores for the control plane, one for queuing, one for crypto, and four each for services and the data plane. The only hardware update required to support hosted services is the inclusion of the 2-TB M.2 NVME SSD drive.

System architecture

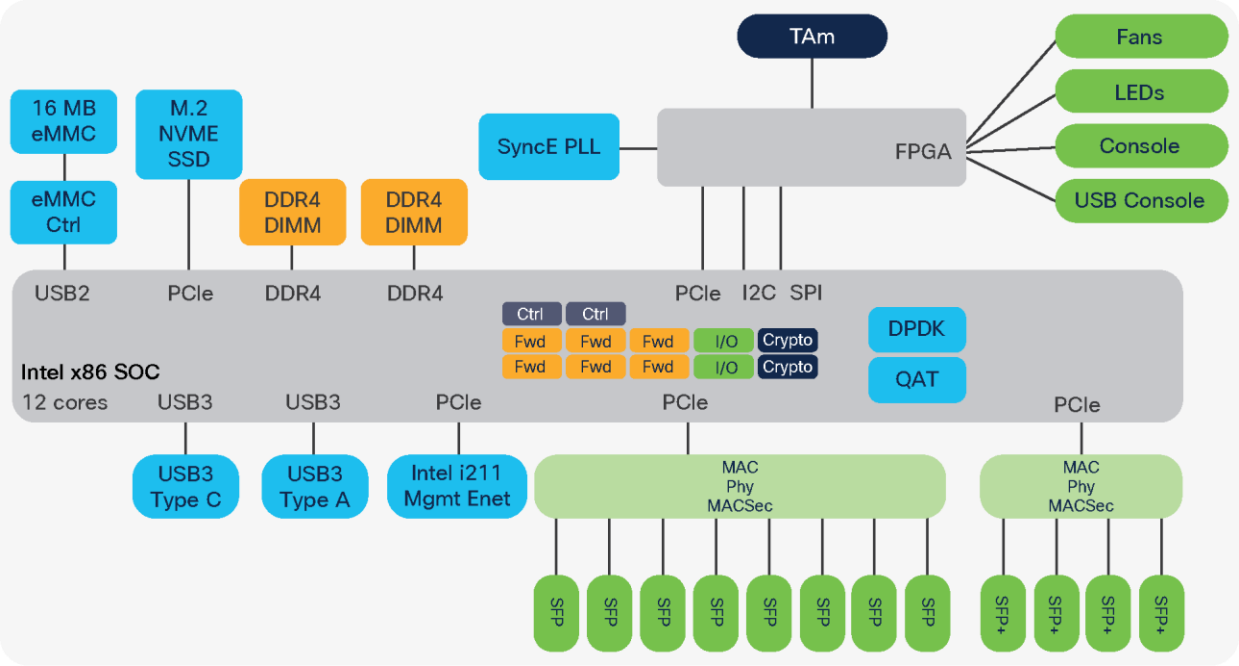

Figure 2.
System architecture

The Intel x86 SoC is the center of the system. The cores are distributed among various functions depending on software configuration. PCIe interfaces are used to interact with the optional storage and the management Ethernet interface, as well as all the data plane-connected Ethernet interfaces. USB is the primary connection mechanism for the bootflash storage. The USB type A and type C ports on the front panel are also directly connected to the x86 SoC. There is also a Field-Programmable Gate Array (FPGA), which is used to interact with fans, LEDs, the RS-232 console, and the USB console port. Lastly, the Trust Anchor module (TAm) provides trustworthy solutions support for the platform. This hardware helps ensure that the Catalyst 8500L platform has a secure boot process and maintains operational security once operational.

Memory and storage

The Catalyst 8500L platform is equipped with 16 GB of bootflash memory for internal storage and a default of 16 GB of DRAM memory for control, data, and services plane operation. The DRAM is upgradable to 32 GB or 64 GB, based on the use case. For additional storage, a 2-TB M2 SATA SSD is available.

Power supply

The Catalyst 8500L platform has a redundant power supply for AC or DC power sources. The AC power supply (PWR-CH1-400WAC) and DC power supply (PWR-CH1-400WDC) each provide 400W of power. The two modules work in load-sharing mode to enable 1 + 1 power supply redundancy. Each power supply module has its own cooling with built-in fans. The DC power supply's input connector is a two-wire screw-type connector.

Chassis cooling

The fan module in the Catalyst 8500L platform is replaceable. It has six fans in total, which are supplied power individually from the power source. This helps the platform achieve N + 1 redundancy such that, if one of the

fans stops working, the remaining fans will continue the cooling function for the chassis. In addition, the fan tray module is field replaceable. The fans in the power supply module are used for cooling the power supply itself, while system-level cooling is provided by the fans within the chassis. The power supply does not depend on the system-level fans for cooling. Fan failure is determined by fan-rotation sensors. The airflow direction is front to back for the chassis as well as for the power supply fans.

Conclusion

The Catalyst 8500L Edge Platform is purpose-built for today's emerging WAN solutions targeting entry-level aggregation and edge throughput. The Catalyst 8500L has a powerful Intel x86 architecture that consolidates a highly efficient data plane, a scalable control plane, cryptography, and an optional services plane. Those distinct edge and aggregation network functions are bundled with a generous set of eight 1G interfaces plus four additional flexible 1G/10G interfaces.

In summary, the Catalyst 8500 and 8500L platforms offer best-in-class hardware with rich software features for high-performance traditional routing and emerging SD-WAN and colocation use cases.

Next steps

More information about the Cisco Catalyst 8500L Edge Platform can be found at the following URLs:

- Cisco Catalyst 8500L Edge Platform
- Cisco Catalyst 8500 Series Edge Platforms

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