Cisco Nexus V9P and V9P-3 FPGA Application SmartNIC

Contents

Highest-density network application card

The Cisco Nexus® V9P and V9P-3 FPGA Application SmartNIC is an FPGA (Field Programmable Gate Array) based network application card, optimized for low latency and high density.

The Cisco Nexus V9P and V9P-3 FPGA Application SmartNIC adapters are equipped with a powerful 16nm Xilinx Virtex UltraScale Plus (VU9P) FPGA with 2.5M logic cells, into a compact, half-height, half-length, PCIe 16x form factor.

High-capacity and low-latency memory

An extensive memory hierarchy for complex, memory-intensive applications.

The Xilinx VU9P FPGA features 75Mbit of block RAM and 270Mbit of UltraRAM on chip. The Cisco Nexus V9P and V9P-3 FPGA Application SmartNIC adapters are also equipped with an additional 9GB of DDR4 DRAM on the board for high throughput access. The DRAM is accessible via a 72-bit-wide bus for maximum performance.

The Cisco Nexus V9P-3 FPGA Application SmartNIC model performs at a higher speed reducing the compile time by 40% over the V9P model compile times, that reduces project build time while increasing network uptime. The improved V9P-3 model logic performance and the faster clocked FPGA helps to eliminate any timing issues and can be programmed to reduce network latency to create a better user experience.

High-bandwidth connectivity

Dual QSFP-DD ports provide up to 400Gbps of full duplex connectivity.

The dual QSFP-DD ports offer high-speed 4x40GbE or 2x200GbE connectivity. Using QSFP-DD breakout cables expands the connectivity to 16x10GbE/25GbE4 connections. This high-density connectivity enables a range of high-performance, directly connected network applications, bypassing the need for traditional switching and multiplexing requirements.

Extensive IP library

Cisco is a specialist in low-latency, high-performance FPGA IP cores.

We provide you the same high-speed, low-latency IP blocks used in our market leading products, including:

- 10GbE PCS/MAC with ultra-low-latency performance
- Low-latency, high-throughput PCIe DMA engine
- Timing, signaling, and register interfaces, including I2C
- Packet field extractor and frame multiplexer (with source code)
- Asynchronous FIFO and CDC modules (with source code)

Several example designs are also provided to help get design work started and completed quickly.

Integrated software library

A standard Linux driver as well as transparent TCP and UDP acceleration and low-level packet access.

The Cisco Nexus V9P and V9P-3 FPGA Application SmartNIC adapters function out of the box as a high-performance network adapter. The entire Cisco Nexus SmartNIC software library is available, including the ExaSOCK sockets application acceleration system and the libexanic direct user-space access API. Libexanic provides easy support for low-latency packet TX/RX, managing the FPGA state (through register access), and low-latency TCP/UDP delegated sending of operations for hybrid hardware/software applications. The Cisco Nexus V9P and V9P-3 FPGA Application SmartNIC adapters also support fast and easy firmware updates (without requiring reboots) and vital statistics monitoring (temperatures, light levels, etc.).

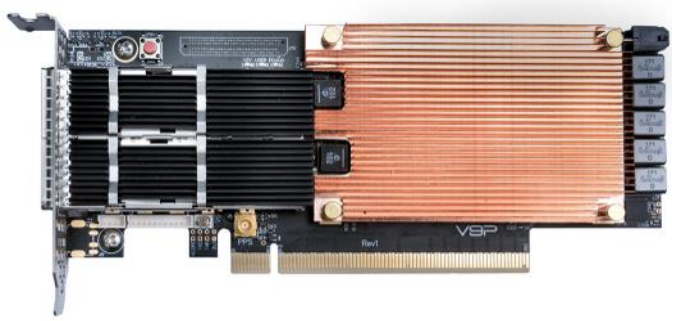

Figure 1.
Cisco Nexus V9P and V9P-3 FPGA Application SmartNIC adapter

Hardware

16nm Xilinx Virtex UltraScale+ FPGA:

- V9P XCVU9P-2, V9P-3 XCVU9P-3
- 2.5M System Logic Cells, 2.3M CLBs
- 2Mb total block RAM
- 270Mb UltraRAM
- 32x 32.75Gb/s I/O transceivers (16 connected to QSFP-DDs, 16 connected to PCIe)

DDR4 DRAM:

- 9GBytes
- 72-bit interface, up to 2666MHz

Oscillators:

- 161MHz crystal
- 10MHz temperature compensated crystal
- 10MHz – 750Hz programmable (I2C) crystal

Input/output:

- PPS in/out via MCX connector, 3.3V CMOS, selectable 50ohm termination
- 8x 1.8V CMOS GPIO via header
- 2x bi-color port LEDs
- 12V external supply (GPU adapter) for >75W designs

Programming/debugging:

- Software-based PCIe flash programming utility
- USB to JTAG port
- JTAG header onboard (auto select)
- 1Gbit onboard flash

Performance

PCS/MAC (TX + RX)[2]:

- 6.2ns (min) @ 10Gbps
- 1Gbps/100Mbps also supported

SERDES/PCS/MAC/CDC (TX+RX):

- Packet trigger, 34ns (min)[2]
- Full loopback, 50ns (min)

Software latency (raw frame, ½RTT)[1]:

- 64 bytes – 816ns
- 256 bytes – 1027ns

General

Form factor:

- Low-profile PCI Express Card
- 168x69mm (6.6x2.7in)

Environmental:

- SmartNIC operating temperature: 0 °C to 55 °C
- SmartNIC storage temperature: -40 °C to 70 °C
- FPGA operating temperature: 0 °C to 100 °C
- Operating Relative Humidity: 5% to 90% (non-condensing)
- Storage Relative Humidity: 5% to 95% (non-condensing)

Ports:

- 2x QSFP-DD
- SMA for PPS in/out

Host interface[3]:

- PCIe x16 Gen 3 @ 8.0 GT/s per lane

Data rates[4]:

- 200GbE, 100GbE, 50GbE, 40GbE, 25GbE, 10GbE, 1GbE, 100M Fast Ethernet

Supported media[4]:

- Fiber (100GBASE-SR4, 100GBASE-LR4, 40GBASE-SR4, 40GBASE-LR4), QSFP/28 Direct Attach breakout

Note: Suitable forced air cooling is required to operate this product.

Product Sustainability

Information about Cisco's environmental, social, and governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability reporting.

Table 1. Cisco environmental sustainability information

Sustainability topic		Reference
General	Information on product-material-content laws and regulations	Materials
	Information on electronic waste laws and regulations, including our products, batteries, and packaging	WEEE Compliance
	Information on product takeback and reuse program	Cisco Takeback and Reuse Program
	Sustainability inquiries	Contact: csr_inquiries@cisco.com
	Environmental	General_Environmental
Material	Product packaging weight and materials	Contact: environment@cisco.com
	Form Factor	General_Form

Cisco Capital

Flexible payment solutions to help you achieve your objectives

Cisco Capital® makes it easier to get the right technology to achieve your objectives, enable business transformation and help you stay competitive. We can help you reduce the total cost of ownership, conserve capital, and accelerate growth. In more than 100 countries, our flexible payment solutions can help you acquire hardware, software, services and complementary third-party equipment in easy, predictable payments. Learn more.

Footnotes:

1. Preliminary results only. Final results to be confirmed.

2. RX + TX time for PMA + PCS + MAC + CDC performing packet trigger based on first data word (for example, dst MAC).

3. Only 8 lanes are exposed at the moment. So, V9P comes up as PCIe Gen 3x8.

4. 25/50/100GbE functionality would need firmware upgrade when available.

Americas Headquarters
Cisco Systems, Inc.
San Jose, CA

Asia Pacific Headquarters
Cisco Systems (USA) Pte. Ltd.
Singapore

Europe Headquarters
Cisco Systems International BV Amsterdam,
The Netherlands

Cisco has more than 200 offices worldwide. Addresses, phone numbers, and fax numbers are listed on the Cisco Website at **https://www.cisco.com/go/offices**.

Printed in USA C78-743830-04 12/21