Cisco Nexus K35-Q FPGA SmartNIC

Contents

Ultra-low latency network interface card

High port density

Dual QSFP+ ports in a half-height form factor provide eight 10GbE interfaces.

The Cisco Nexus K35-Q FPGA SmartNIC is a 10/40Gbps interface card specifically optimized for low-latency environments. Through the use of QSFP+ breakout cables, it can connect to eight SFP+ ports. This enables a range of high-performance applications such as packet capture across multiple connections, or market data line arbitration across many different feeds.

Easy to use

In addition to a standard Linux driver, a transparent TCP and UDP acceleration library is included, as well as a library for low-level access.

A transparent socket acceleration library allows applications to benefit from the low latency of a kernel bypass, in most cases without modifications to the applications. For the most latency sensitive applications, a library called "libexanic" allows direct low-level access to the Cisco Nexus K35-Q FPGA SmartNIC hardware and includes simple functions for sending and receiving Ethernet frames. With the optional firmware development kit, it is even possible to extend the SmartNIC firmware and add your own logic to the onboard Field Programmable Gate Array (FPGA).

Advanced capture

Flow steering delivers packets to the right application's receive buffer.

Filters can be defined over Ethernet frame components such as SRC/DST MAC, SRC/DST IP, etc., and a receive buffer associated with that filter. As packets come off the wire, the Cisco Nexus K35-Q FPGA SmartNIC will analyze the traffic and deliver packets that the match filters directly to the correct receive buffer. Nonmatched packets are delivered to the default buffer. This flow steering is done inline at line rate, adding no additional latency. Flow hashing distributes packets evenly across multiple buffers, allowing CPU load to be spread for demanding capture and analysis applications.

Timestamping

Built-in timestamping functionality records each frame's arrival time to within 6.2ns.

These timestamps are available through a direct API and through Exact Capture, our free and open-source, high-rate capture system. Exact Capture can write tcpdump-compatible captures at line-rate to disk.

Additionally, the Cisco Nexus K35-Q FPGA SmartNIC features Pulse-Per-Second (PPS) input and output and supports hardware accelerated PTP. These can be used to synchronize the SmartNIC clock to external time references (such as a GPS receivers), allowing users to meaningfully compare captured timestamps across multiple servers and geographic locations.

Figure 1.
Cisco Nexus K35-Q FPGA SmartNIC

Performance

Typical latency, raw frames:[1]

- 64 bytes: 800 ns
- 256 bytes: 1.02 μs

Typical latency, raw frames with preloaded TX buffer:[1]

- 64 bytes: 730 ns
- 256 bytes: 950 ns

Typical latency, UDP:[2]

- 14 bytes: 900 ns
- 256 bytes: 1.22 μs

Typical latency, TCP:[2]

- 14 bytes: 950 ns
- 256 bytes: 1.22 μs

Timestamping

Timestamp resolution:

- 6.2ns

Timestamp availability:

- All received frames, most recently transmitted frame

Time synchronization:

- Host, hardware assisted PTP, optional PPS

PPS input/output:

- 3.3V CMOS, selectable 50ohm termination

Footnotes

[1] Latencies are median latencies for raw frames from wire-user space-wire via the libexanic library, on a 3.5Ghz Intel® Ivy Bridge processor.

[2] Latencies are median half round trip time latencies for the sockperf benchmark using the exasock socket Acceleration Library. More information about benchmarking methodology is available on request.

General

Form factor:

- Low-profile PCI Express Card
- 150x68mm (5.9x2.67in)

Environmental:

- Operating temperature: 0 °C to 55 °C
- Storage temperature: -40 °C to 70 °C
- Operating Relative Humidity: 5% to 90% (non-condensing)
- Storage Relative Humidity: 5% to 95% (non-condensing)

Ports:

- 2x QSFP+
- SMA for PPS in/out

Data rates:

- 40GbE, 10GbE, 1GbE, 100M Fast Ethernet

Supported media:

- Fiber (10GBASE-SR, 10GBASE-LR, 1000BASE-SX), SFP+ Direct Attach

Host interface:

- PCIe x8 Gen 3 @ 8.0 GT/s per lane

Operating systems:

- Linux x86_64 (all distributions)

Other features

Flow steering:

- 128 IP rules per port
- 64 MAC rules per port

Capture:

- Line-rate capture to disk

FPGA Development Kit:

- Add custom user logic to FPGA
- Xilinx UltraScale XCKU035-2
- Fully integrated with drivers, utilities, and TCP/UDP stack

Product sustainability

Information about Cisco's Environmental, Social and Governance (ESG) initiatives and performance is provided in Cisco's CSR and sustainability reporting.

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