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1.7 jansson 2.9

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1.8 libxml2 2.9.12

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1.9 libmspack 0.10.1alpha

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1.10 nghttp2 1.47.0

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set yrange [0:]

set terminal pngcairo font 'Sans, 8' lw 1 size 1400,1024

set xtics rotate by -45

set style histogram errorbars gap 2 lw 1

set style fill solid border -1

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* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/tinystr.cpp

* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/tinystr.h

No license file was found, but licenses were detected in source scan.

/*

www.sourceforge.net/projects/tinyxml

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*/

Found in path(s):

```
* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/tinyxmlerror.cpp
```

No license file was found, but licenses were detected in source scan.

```
/*
```

www.sourceforge.net/projects/tinyxml

Original code by Lee Thomason (www.grinninglizard.com)

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```
*/
```

Found in path(s):

```
* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/tinyxmlparser.cpp
```

No license file was found, but licenses were detected in source scan.

```
/** @mainpage
```

```
<h1> TinyXML </h1>
```

TinyXML is a simple, small, C++ XML parser that can be easily integrated into other programs.

```
<h2> What it does. </h2>
```

In brief, TinyXML parses an XML document, and builds from that a Document Object Model (DOM) that can be read, modified, and saved.

XML stands for "eXtensible Markup Language." It allows you to create your own document markups. Where HTML does a very good job of marking documents for browsers, XML allows you to define any kind of document markup, for example a document that describes a "to do" list for an organizer application. XML is a very structured and convenient format.

All those random file formats created to store application data can all be replaced with XML. One parser for everything.

The best place for the complete, correct, and quite frankly hard to read spec is at <http://www.w3.org/TR/2004/REC-xml-20040204/>. An intro to XML (that I really like) can be found at <http://skew.org/xml/tutorial/>.

There are different ways to access and interact with XML data. TinyXML uses a Document Object Model (DOM), meaning the XML data is parsed into a C++ objects that can be browsed and manipulated, and then written to disk or another output stream. You can also construct an XML document from scratch with C++ objects and write this to disk or another output stream.

TinyXML is designed to be easy and fast to learn. It is two headers and four cpp files. Simply add these to your project and off you go. There is an example file - xmltest.cpp - to get you started.

TinyXML is released under the ZLib license, so you can use it in open source or commercial code. The details of the license are at the top of every source file.

TinyXML attempts to be a flexible parser, but with truly correct and compliant XML output. TinyXML should compile on any reasonably C++ compliant system. It does not rely on exceptions or RTTI. It can be compiled with or without STL support. TinyXML fully supports the UTF-8 encoding, and the first 64k character entities.

<h2> What it doesn't do. </h2>

TinyXML doesn't parse or use DTDs (Document Type Definitions) or XSLs (eXtensible Stylesheet Language.) There are other parsers out there (check out www.sourceforge.org, search for XML) that are much more fully featured. But they are also much bigger, take longer to set up in your project, have a higher learning curve, and often have a more restrictive license. If you are working with browsers or have more complete XML needs, TinyXML is not the parser for you.

The following DTD syntax will not parse at this time in TinyXML:

```
@verbatim
<!DOCTYPE Archiv [
  <!ELEMENT Comment (#PCDATA)>
]>
@endverbatim
```

because TinyXML sees this as a !DOCTYPE node with an illegally embedded !ELEMENT node. This may be addressed in the future.

<h2> Tutorials. </h2>

For the impatient, here is a tutorial to get you going. A great way to get started, but it is worth your time to read this (very short) manual completely.

- @subpage tutorial0

<h2> Code Status. </h2>

TinyXML is mature, tested code. It is very stable. If you find bugs, please file a bug report on the sourceforge web site (www.sourceforge.net/projects/tinyxml). We'll get them straightened out as soon as possible.

There are some areas of improvement; please check sourceforge if you are interested in working on TinyXML.

<h2> Related Projects </h2>

TinyXML projects you may find useful! (Descriptions provided by the projects.)

 TinyXPath (<http://tinyxpath.sourceforge.net>). TinyXPath is a small footprint XPath syntax decoder, written in C++.

 TinyXML++ (<http://code.google.com/p/ticpp/>). TinyXML++ is a completely new interface to TinyXML that uses MANY of the C++ strengths. Templates, exceptions, and much better error handling.

<h2> Features </h2>

<h3> Using STL </h3>

TinyXML can be compiled to use or not use STL. When using STL, TinyXML uses the std::string class, and fully supports std::istream, std::ostream, operator<<, and operator>>. Many API methods have both 'const char*' and 'const std::string&' forms.

When STL support is compiled out, no STL files are included whatsoever. All the string classes are implemented by TinyXML itself. API methods all use the 'const char*' form for input.

Use the compile time #define:

TIXML_USE_STL

to compile one version or the other. This can be passed by the compiler, or set as the first line of "tinyxml.h".

Note: If compiling the test code in Linux, setting the environment variable TINYXML_USE_STL=YES/NO will control STL compilation. In the Windows project file, STL and non STL targets are provided. In your project, It's probably easiest to add the line "#define TIXML_USE_STL" as the first line of tinyxml.h.

<h3> UTF-8 </h3>

TinyXML supports UTF-8 allowing to manipulate XML files in any language. TinyXML also supports "legacy mode" - the encoding used before UTF-8 support and probably best described as "extended ascii".

Normally, TinyXML will try to detect the correct encoding and use it. However, by setting the value of TIXML_DEFAULT_ENCODING in the header file, TinyXML can be forced to always use one encoding.

TinyXML will assume Legacy Mode until one of the following occurs:

 If the non-standard but common "UTF-8 lead bytes" (0xef 0xbb 0xbf) begin the file or data stream, TinyXML will read it as UTF-8.

 If the declaration tag is read, and it has an encoding="UTF-8", then TinyXML will read it as UTF-8.

 If the declaration tag is read, and it has no encoding specified, then TinyXML will read it as UTF-8.

 If the declaration tag is read, and it has an encoding="something else", then TinyXML will read it as Legacy Mode. In legacy mode, TinyXML will work as it did before. It's not clear what that mode does exactly, but old content should keep working.

 Until one of the above criteria is met, TinyXML runs in Legacy Mode.

What happens if the encoding is incorrectly set or detected? TinyXML will try to read and pass through text seen as improperly encoded. You may get some strange results or mangled characters. You may want to force TinyXML to the correct mode.

You may force TinyXML to Legacy Mode by using LoadFile(TIXML_ENCODING_LEGACY) or LoadFile(filename, TIXML_ENCODING_LEGACY). You may force it to use legacy mode all the time by setting TIXML_DEFAULT_ENCODING = TIXML_ENCODING_LEGACY. Likewise, you may force it to TIXML_ENCODING_UTF8 with the same technique.

For English users, using English XML, UTF-8 is the same as low-ASCII. You don't need to be aware of UTF-8 or change your code in any way. You can think of UTF-8 as a "superset" of ASCII.

UTF-8 is not a double byte format - but it is a standard encoding of Unicode!
TinyXML does not use or directly support wchar, TCHAR, or Microsoft's _UNICODE at this time.
It is common to see the term "Unicode" improperly refer to UTF-16, a wide byte encoding of unicode. This is a source of confusion.

For "high-ascii" languages - everything not English, pretty much - TinyXML can handle all languages, at the same time, as long as the XML is encoded in UTF-8. That can be a little tricky, older programs and operating systems tend to use the "default" or "traditional" code page. Many apps (and almost all modern ones) can output UTF-8, but older or stubborn (or just broken) ones still output text in the default code page.

For example, Japanese systems traditionally use SHIFT-JIS encoding.
Text encoded as SHIFT-JIS can not be read by TinyXML.
A good text editor can import SHIFT-JIS and then save as UTF-8.

The `Skew.org link` does a great job covering the encoding issue.

The test file "utf8test.xml" is an XML containing English, Spanish, Russian, and Simplified Chinese. (Hopefully they are translated correctly). The file "utf8test.gif" is a screen capture of the XML file, rendered in IE. Note that if you don't have the correct fonts (Simplified Chinese or Russian) on your system, you won't see output that matches the GIF file even if you can parse it correctly. Also note that (at least on my Windows machine) console output is in a Western code page, so that Print() or printf() cannot correctly display the file. This is not a bug in TinyXML - just an OS issue. No data is lost or destroyed by TinyXML. The console just doesn't render UTF-8.

`<h3> Entities </h3>`

TinyXML recognizes the pre-defined "character entities", meaning special characters. Namely:

```
@verbatim
&amp; &
&lt; <
&gt; >
&quot; "
&apos; '
@endverbatim
```

These are recognized when the XML document is read, and translated to there UTF-8 equivalents. For instance, text with the XML of:

```
@verbatim
Far &amp; Away
@endverbatim
```

will have the Value() of "Far & Away" when queried from the TiXmlText object, and will be written back to the XML stream/file as an ampersand. Older versions of TinyXML "preserved" character entities, but the newer versions will translate them into characters.

Additionally, any character can be specified by its Unicode code point:

The syntax " " or " " are both to the non-breaking space character.

<h3> Printing </h3>

TinyXML can print output in several different ways that all have strengths and limitations.

- Print(FILE*). Output to a std-C stream, which includes all C files as well as stdout.
 - "Pretty prints", but you don't have control over printing options.
 - The output is streamed directly to the FILE object, so there is no memory overhead in the TinyXML code.
 - used by Print() and SaveFile()
- operator<<. Output to a c++ stream.
 - Integrates with standart C++ iostreams.
 - Outputs in "network printing" mode without line breaks. Good for network transmission and moving XML between C++ objects, but hard for a human to read.
- TiXmlPrinter. Output to a std::string or memory buffer.
 - API is less concise
 - Future printing options will be put here.
 - Printing may change slightly in future versions as it is refined and expanded.

<h3> Streams </h3>

With TIXML_USE_STL on TinyXML supports C++ streams (operator <<, >>) streams as well as C (FILE*) streams. There are some differences that you may need to be aware of.

C style output:

- based on FILE*
- the Print() and SaveFile() methods

Generates formatted output, with plenty of white space, intended to be as human-readable as possible. They are very fast, and tolerant of ill formed XML documents. For example, an XML document that contains 2 root elements and 2 declarations, will still print.

C style input:

- based on FILE*
- the Parse() and LoadFile() methods

A fast, tolerant read. Use whenever you don't need the C++ streams.

C++ style output:

- based on `std::ostream`
- `operator<<`

Generates condensed output, intended for network transmission rather than readability. Depending on your system's implementation of the `ostream` class, these may be somewhat slower. (Or may not.) Not tolerant of ill formed XML: a document should contain the correct one root element. Additional root level elements will not be streamed out.

C++ style input:

- based on `std::istream`
- `operator>>`

Reads XML from a stream, making it useful for network transmission. The tricky part is knowing when the XML document is complete, since there will almost certainly be other data in the stream. TinyXML will assume the XML data is complete after it reads the root element. Put another way, documents that are ill-constructed with more than one root element will not read correctly. Also note that `operator>>` is somewhat slower than `Parse`, due to both implementation of the STL and limitations of TinyXML.

<h3> White space </h3>

The world simply does not agree on whether white space should be kept, or condensed. For example, pretend the '_' is a space, and look at "Hello___world". HTML, and at least some XML parsers, will interpret this as "Hello_world". They condense white space. Some XML parsers do not, and will leave it as "Hello___world". (Remember to keep pretending the _ is a space.) Others suggest that ___Hello___world___ should become Hello___world.

It's an issue that hasn't been resolved to my satisfaction. TinyXML supports the first 2 approaches. Call `TiXmlBase::SetCondenseWhiteSpace(bool)` to set the desired behavior. The default is to condense white space.

If you change the default, you should call `TiXmlBase::SetCondenseWhiteSpace(bool)` before making any calls to `Parse` XML data, and I don't recommend changing it after it has been set.

<h3> Handles </h3>

Where browsing an XML document in a robust way, it is important to check for null returns from method calls. An error safe implementation can generate a lot of code like:

```
@verbatim
TiXmlElement* root = document.FirstChildElement( "Document" );
if ( root )
{
```

```

TiXmlElement* element = root->FirstChildElement( "Element" );
if ( element )
{
    TiXmlElement* child = element->FirstChildElement( "Child" );
    if ( child )
    {
        TiXmlElement* child2 = child->NextSiblingElement( "Child" );
        if ( child2 )
        {
            // Finally do something useful.
        }
    }
}
@endverbatim

```

Handles have been introduced to clean this up. Using the `TiXmlHandle` class, the previous code reduces to:

```

@verbatim
TiXmlHandle docHandle( &document );
TiXmlElement* child2 = docHandle.FirstChild( "Document" ).FirstChild( "Element" ).Child( "Child", 1
).ToElement();
if ( child2 )
{
    // do something useful
}
@endverbatim

```

Which is much easier to deal with. See `TiXmlHandle` for more information.

<h3> Row and Column tracking </h3>

Being able to track nodes and attributes back to their origin location in source files can be very important for some applications. Additionally, knowing where parsing errors occurred in the original source can be very time saving.

TinyXML can track the row and column origin of all nodes and attributes in a text file. The `TiXmlBase::Row()` and `TiXmlBase::Column()` methods return the origin of the node in the source text. The correct tabs can be configured in `TiXmlDocument::SetTabSize()`.

<h2> Using and Installing </h2>

To Compile and Run xmltest:

A Linux Makefile and a Windows Visual C++ .dsw file is provided. Simply compile and run. It will write the file `demotest.xml` to your disk and generate output on the screen. It also tests walking the DOM by printing out the number of nodes found using different techniques.

The Linux makefile is very generic and runs on many systems - it is currently tested on mingw and MacOSX. You do not need to run 'make depend'. The dependencies have been hard coded.

<h3>Windows project file for VC6</h3>

tinyxml: tinyxml library, non-STL

tinyxmlSTL: tinyxml library, STL

tinyXmlTest: test app, non-STL

tinyXmlTestSTL: test app, STL

<h3>Makefile</h3>

At the top of the makefile you can set:

PROFILE, DEBUG, and TINYXML_USE_STL. Details (such that they are) are in the makefile.

In the tinyxml directory, type "make clean" then "make". The executable file 'xmltest' will be created.

<h3>To Use in an Application:</h3>

Add tinyxml.cpp, tinyxml.h, tinyxmlerror.cpp, tinyxmlparser.cpp, tinystr.cpp, and tinystr.h to your project or make file. That's it! It should compile on any reasonably compliant C++ system. You do not need to enable exceptions or RTTI for TinyXML.

<h2>How TinyXML works. </h2>

An example is probably the best way to go. Take:

@verbatim

```
<?xml version="1.0" standalone=no>
```

```
<!-- Our to do list data -->
```

```
<ToDo>
```

```
<Item priority="1"> Go to the <b>Toy store!</b></Item>
```

```
<Item priority="2"> Do bills</Item>
```

```
</ToDo>
```

@endverbatim

Its not much of a To Do list, but it will do. To read this file (say "demo.xml") you would create a document, and parse it in:

@verbatim

```
TiXmlDocument doc( "demo.xml" );
doc.LoadFile();
@endverbatim
```

And its ready to go. Now lets look at some lines and how they relate to the DOM.

```
@verbatim
<?xml version="1.0" standalone=no>
@endverbatim
```

The first line is a declaration, and gets turned into the TiXmlDeclaration class. It will be the first child of the document node.

This is the only directive/special tag parsed by TinyXML. Generally directive tags are stored in TiXmlUnknown so the commands wont be lost when it is saved back to disk.

```
@verbatim
<!-- Our to do list data -->
@endverbatim
```

A comment. Will become a TiXmlComment object.

```
@verbatim
<ToDo>
@endverbatim
```

The "ToDo" tag defines a TiXmlElement object. This one does not have any attributes, but does contain 2 other elements.

```
@verbatim
<Item priority="1">
@endverbatim
```

Creates another TiXmlElement which is a child of the "ToDo" element. This element has 1 attribute, with the name "priority" and the value "1".

```
@verbatim
Go to the
@endverbatim
```

A TiXmlText. This is a leaf node and cannot contain other nodes. It is a child of the "Item" TiXmlElement.

```
@verbatim
```

```
<bold>  
@endverbatim
```

Another TiXmlElement, this one a child of the "Item" element.

Etc.

Looking at the entire object tree, you end up with:

```
@verbatim  
TiXmlDocument  "demo.xml"  
TiXmlDeclaration "version='1.0'" "standalone=no"  
TiXmlComment   " Our to do list data"  
TiXmlElement   "ToDo"  
TiXmlElement   "Item" Attributes: priority = 1  
  TiXmlText    "Go to the "  
  TiXmlElement "bold"  
  TiXmlText    "Toy store!"  
TiXmlElement   "Item" Attributes: priority=2  
  TiXmlText    "Do bills"  
@endverbatim
```

```
<h2> Documentation </h2>
```

The documentation is build with Doxygen, using the 'dox' configuration file.

```
<h2> License </h2>
```

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distribution.

<h2> References </h2>

The World Wide Web Consortium is the definitive standard body for XML, and their web pages contain huge amounts of information.

The definitive spec: http://www.w3.org/TR/2004/REC-xml-20040204/

I also recommend "XML Pocket Reference" by Robert Eckstein and published by OReilly...the book that got the whole thing started.

<h2> Contributors, Contacts, and a Brief History </h2>

Thanks very much to everyone who sends suggestions, bugs, ideas, and encouragement. It all helps, and makes this project fun. A special thanks to the contributors on the web pages that keep it lively.

So many people have sent in bugs and ideas, that rather than list here we try to give credit due in the "changes.txt" file.

TinyXML was originally written by Lee Thomason. (Often the "I" still in the documentation.) Lee reviews changes and releases new versions, with the help of Yves Berquin, Andrew Ellerton, and the tinyXml community.

We appreciate your suggestions, and would love to know if you use TinyXML. Hopefully you will enjoy it and find it useful. Please post questions, comments, file bugs, or contact us at:

www.sourceforge.net/projects/tinyxml

Lee Thomason, Yves Berquin, Andrew Ellerton
*/

Found in path(s):

* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/readme.txt

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Found in path(s):

* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/docs/tinyxml_8h_source.html

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Found in path(s):

* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/docs/tinystr_8h_source.html

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/*

www.sourceforge.net/projects/tinyxml

Original code by Lee Thomason (www.grinninglizard.com)

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*/

Found in path(s):

* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/tinyxml.cpp

* /opt/cola/permits/1222902257_1637000982.24/0/tinyxml-2-6-2-zip/tinyxml/tinyxml.h

1.12 mbed-tls 2.23.133

1.12.1 Available under license :

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1.13 pcre 10.37

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 ; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
 ; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

```

define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
; CHECK-LABEL: PR41535:
; CHECK:      // %bb.0:
; CHECK-NEXT:  ext v0.8b, v0.8b, v1.8b, #4
; CHECK-NEXT:  mov v0.d[1], v0.d[0]
; CHECK-NEXT:  ret
%cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
%cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
  
```

```

%r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
ret <4 x i32> %r
}
; RUN: llc <%s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.

define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
%L34 = load i8, i8* %0
%Cmp56 = icmp sgt i8 undef, %L34
br label %CF246

CF246:                                ; preds = %CF246, %BB
%S1163 = select i1 %Cmp56, i8 %L34, i8 undef
br i1 undef, label %CF246, label %CF248

CF248:                                ; preds = %CF248, %CF246
store i8 %S1163, i8* %0
br label %CF248
}

```

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```
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --
check-attributes --check-globals
```

```
; RUN: opt -attributor -enable-new-pm=0 -attributor-manifest-internal -attributor-max-iterations-verify -attributor-
annotate-decl-cs -attributor-max-iterations=6 -S < %s | FileCheck %s --check-
prefixes=CHECK,NOT_CGSCC_NPM,NOT_CGSCC_OPM,NOT_TUNIT_NPM,IS__TUNIT____,IS_______OP
M,IS__TUNIT_OPM
```

```
; RUN: opt -aa-pipeline=basic-aa -passes=attributor -attributor-manifest-internal -attributor-max-iterations-verify -
attributor-annotate-decl-cs -attributor-max-iterations=6 -S < %s | FileCheck %s --check-
prefixes=CHECK,NOT_CGSCC_OPM,NOT_CGSCC_NPM,NOT_TUNIT_OPM,IS__TUNIT____,IS_______NP
M,IS__TUNIT_NPM
```

```
; RUN: opt -attributor-cgsc -enable-new-pm=0 -attributor-manifest-internal -attributor-annotate-decl-cs -S < %s |
FileCheck %s --check-
prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_NPM,IS__CGSCC____,IS_______OP
M,IS__CGSCC_OPM
```

```
; RUN: opt -aa-pipeline=basic-aa -passes=attributor-cgsc -attributor-manifest-internal -attributor-annotate-decl-cs -
S < %s | FileCheck %s --check-
prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_OPM,IS__CGSCC____,IS_______NP
M,IS__CGSCC_NPM
```

```
; Test that we only promote arguments when the caller/callee have compatible
```

```
; function attributes.
```

```
target triple = "x86_64-unknown-linux-gnu"
```

```

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR0:[0-9]+]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:  ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0:[0-9]+]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:  ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0:[0-9]+]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:  ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn

```

```

; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_OPM-SAME: (<8 x i64>* norecapture norefree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* norecapture norefree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]
; IS__TUNIT_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* norecapture norefree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* norecapture norefree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7:[0-9]+]]
; IS__TUNIT_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT:  ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint norefree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* norecapture norefree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* norecapture norefree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]
; IS__TUNIT_NPM-NEXT:  [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias norecapture norefree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7:[0-9]+]]
; IS__TUNIT_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:  ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norefree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME: (<8 x i64>* norecapture norefree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR0]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:  [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:  call void @llvm.memset.p0i8.i64(i8* norecapture norefree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]
; IS__CGSCC_OPM-NEXT:  call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* norecapture norefree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* norecapture norefree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7:[0-9]+]]
; IS__CGSCC_OPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

```

```

; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR0]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7:[0-9]+]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1:[0-9]+]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT: ret void
;

```

```

; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{[[@+]]}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1:[0-9]+]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{[[@+]]}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1:[0-9]+]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {[[@+]]}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void

```



```

;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^\@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture norecurse
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^\@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture norecurse noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^\@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void

```

```

@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT:  [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:  ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:  ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256

```

```

; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocardture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocardture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocardture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocardture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocardture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocardture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocardture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocardture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

```

```

; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR0]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapture norecurse noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR0]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture norecurse
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2

```

```

ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{[[@+]}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR0]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:  ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{[[@+]}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:  ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{[[@+]}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT:  [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:  ret void
;
bb:
  %tmp = load <8 x i64>, <8 x i64>* %arg1
  store <8 x i64> %tmp, <8 x i64>* %arg
  ret void
}

```

```

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture norecurse noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture norecurse
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture norecurse noundef

```

```

nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]] #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{{^@+}}} @avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{{^@+}}} @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64

```

```

; IS_____OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT: ret void
;
; IS_____NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____NPM-LABEL: define
{[^[^@]+]}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS_____NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree noundef nonnull readonly align 64
dereferenceable(64) [[ARG1:%.*]]) #[[ATTR1:[0-9]+]] {
; IS_____NPM-NEXT: bb:
; IS_____NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {[^[^@]+]}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {[^[^@]+]}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]

```



```

; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{^[^@]+}} @avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{^[^@]+}} @avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*

```

```

call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #2 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR2:[0-9]+]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:  ret void
;
; IS_____NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____NPM-LABEL: define
{{{^@+}}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS_____NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree noundef nonnull readonly align 64
dereferenceable(64) [[ARG1:%.*]]) #[[ATTR2:[0-9]+]] {
; IS_____NPM-NEXT: bb:
; IS_____NPM-NEXT:  [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____NPM-NEXT:  store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____NPM-NEXT:  ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
;
; IS__TUNIT__OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT__OPM-LABEL: define {{{^@+}}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__TUNIT__OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT__OPM-NEXT: bb:
; IS__TUNIT__OPM-NEXT:  [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT__OPM-NEXT:  [[TMP2:%.*]] = alloca <8 x i64>, align 32

```

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; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture norecurse noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^\@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture norecurse
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture norecurse noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^\@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture norecurse noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^\@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256

```

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; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #3 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define {{{^@+}}} @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR3:[0-9]+]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{{^@+}}} @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3:[0-9]+]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64

```

```

; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^\@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture norecurse noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3:[0-9]+]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^\@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* nocapture norecurse noundef nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly align 64
dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^\@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

```

```

; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse nosync nounwind uwtable willreturn
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture norecurse nosync nounwind uwtable willreturn
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{^[^@]+}} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture norecurse nosync nounwind uwtable willreturn align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse nosync nounwind uwtable willreturn
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture norecurse nosync nounwind uwtable willreturn
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse nosync nounwind uwtable willreturn align 64
dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{^[^@]+}} @avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture norecurse nosync nounwind uwtable willreturn align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse nosync nounwind uwtable willreturn
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture norecurse nosync nounwind uwtable willreturn
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32

```

```

%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

; This should promote

```

define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #4 {

```

```

;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define {{{^@+}}} @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR4:[0-9]+]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{{^@+}}} @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR4]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{{^@+}}} @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR4]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1

```

```

store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^\@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR3]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* nocapture norecurse noundef nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noundef nonnull readonly align 64
dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^\@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture norecurse writeonly [[ARG:%.*]]) #[[ATTR3]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture norecurse noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^\@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture norecurse noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR3]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

```



```

; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noalias nounwind writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* nocapture norecurse noalias nounwind
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture norecurse noalias nounwind readonly align 64
dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {@llvm.arch} @avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture norecurse noalias nounwind writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR3]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture norecurse noalias nounwind writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture norecurse noalias
nounwind writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-

```

```

width="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
;
; IS__TUNIT____: attributes #[[ATTR0:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-features"="+avx512vl" }
; IS__TUNIT____: attributes #[[ATTR1:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__TUNIT____: attributes #[[ATTR2:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__TUNIT____: attributes #[[ATTR3:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__TUNIT____: attributes #[[ATTR4:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__TUNIT____: attributes #[[ATTR5:[0-9]+]] = { argmemonly norecurse nounwind willreturn writeonly }
; IS__TUNIT____: attributes #[[ATTR6:[0-9]+]] = { willreturn writeonly }
; IS__TUNIT____: attributes #[[ATTR7:[0-9]+]] = { norecurse nosync nounwind willreturn }
;
; IS__CGSCC____: attributes #[[ATTR0:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-features"="+avx512vl" }
; IS__CGSCC____: attributes #[[ATTR1:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__CGSCC____: attributes #[[ATTR2:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__CGSCC____: attributes #[[ATTR3:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__CGSCC____: attributes #[[ATTR4:[0-9]+]] = { argmemonly inlinehint norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__CGSCC____: attributes #[[ATTR5:[0-9]+]] = { argmemonly norecurse nounwind willreturn writeonly }
; IS__CGSCC____: attributes #[[ATTR6:[0-9]+]] = { willreturn writeonly }
; IS__CGSCC____: attributes #[[ATTR7:[0-9]+]] = { nounwind willreturn }
;
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -scalarize-masked-mem-intrin -S <%s | FileCheck %s

; Testing that masked gathers operating on scalable vectors that are
; packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv4i32(
; CHECK: call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32
define <vscale x 4 x i32> @masked_gather_nxv4i32(<vscale x 4 x i32*> %ld, <vscale x 4 x i1> %masks, <vscale x
4 x i32> %passthru) {
    %res = call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x i32*> %ld, i32 0, <vscale x 4 x i1>
%.masks, <vscale x 4 x i32> %passthru)
    ret <vscale x 4 x i32> %res
}

```

; Testing that masked gathers operating on scalable vectors of FP data
; that is packed in SVE registers are not scalarized.

```
; CHECK-LABEL: @masked_gather_nxv2f64(  
; CHECK: call <vscale x 2 x double> @llvm.masked.gather.nxv2f64  
define <vscale x 2 x double> @masked_gather_nxv2f64(<vscale x 2 x double*> %ld, <vscale x 2 x i1> %masks,  
<vscale x 2 x double> %passthru) {  
    %res = call <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x double*> %ld, i32 0, <vscale x 2 x  
i1> %masks, <vscale x 2 x double> %passthru)  
    ret <vscale x 2 x double> %res  
}
```

; Testing that masked gathers operating on scalable vectors of FP data
; that is unpacked in SVE registers are not scalarized.

```
; CHECK-LABEL: @masked_gather_nxv2f16(  
; CHECK: call <vscale x 2 x half> @llvm.masked.gather.nxv2f16  
define <vscale x 2 x half> @masked_gather_nxv2f16(<vscale x 2 x half*> %ld, <vscale x 2 x i1> %masks, <vscale  
x 2 x half> %passthru) {  
    %res = call <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x half*> %ld, i32 0, <vscale x 2 x i1>  
%masks, <vscale x 2 x half> %passthru)  
    ret <vscale x 2 x half> %res  
}
```

; Testing that masked gathers operating on 64-bit fixed vectors are
; scalarized because NEON doesn't have support for masked gather
; instructions.

```
; CHECK-LABEL: @masked_gather_v2f32(  
; CHECK-NOT: @llvm.masked.gather.v2f32(  
define <2 x float> @masked_gather_v2f32(<2 x float*> %ld, <2 x i1> %masks, <2 x float> %passthru) {  
    %res = call <2 x float> @llvm.masked.gather.v2f32(<2 x float*> %ld, i32 0, <2 x i1> %masks, <2 x float>  
%passthru)  
    ret <2 x float> %res  
}
```

; Testing that masked gathers operating on 128-bit fixed vectors are
; scalarized because NEON doesn't have support for masked gather
; instructions and because we are not targeting fixed width SVE.

```
; CHECK-LABEL: @masked_gather_v4i32(  
; CHECK-NOT: @llvm.masked.gather.v4i32(  
define <4 x i32> @masked_gather_v4i32(<4 x i32*> %ld, <4 x i1> %masks, <4 x i32> %passthru) {  
    %res = call <4 x i32> @llvm.masked.gather.v4i32(<4 x i32*> %ld, i32 0, <4 x i1> %masks, <4 x i32> %passthru)  
    ret <4 x i32> %res  
}
```

```
declare <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x i32*> %ptrs, i32 %align, <vscale x 4 x i1>
%mask, <vscale x 4 x i32> %passthru)
declare <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x double*> %ptrs, i32 %align, <vscale x
2 x i1> %mask, <vscale x 2 x double> %passthru)
declare <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x half*> %ptrs, i32 %align, <vscale x 2 x
i1> %mask, <vscale x 2 x half> %passthru)
declare <2 x float> @llvm.masked.gather.v2f32(<2 x float*> %ptrs, i32 %align, <2 x i1> %mask, <2 x float>
%passthru)
declare <4 x i32> @llvm.masked.gather.v4i32(<4 x i32*> %ptrs, i32 %align, <4 x i1> %mask, <4 x i32>
%passthru)
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```

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s

;

; D31946

; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.

; Additionally ensure that the output code actually put fp128 values in SSE registers.

```
declare fp128 @llvm.fabs.f128(fp128)
```

```
declare fp128 @llvm.copysign.f128(fp128, fp128)
```

```
define fp128 @TestSelect(fp128 %a, fp128 %b) {
```

```
; CHECK-LABEL: TestSelect:
```

```
; CHECK:      # %bb.0:
```

```
; CHECK-NEXT: pushq %rbx
```

```
; CHECK-NEXT: .cfi_def_cfa_offset 16
```

```
; CHECK-NEXT: subq $32, %rsp
```

```
; CHECK-NEXT: .cfi_def_cfa_offset 48
```

```
; CHECK-NEXT: .cfi_offset %rbx, -16
```

```
; CHECK-NEXT: movaps %xmm1, {[[-0-9]+]}(%r{[sb]})p # 16-byte Spill
```

```
; CHECK-NEXT: movaps %xmm0, (%rsp) # 16-byte Spill
```

```
; CHECK-NEXT: callq __gttf2@PLT
```

```
; CHECK-NEXT: movl %eax, %ebx
```

```
; CHECK-NEXT: movaps (%rsp), %xmm0 # 16-byte Reload
```

```
; CHECK-NEXT: movaps {[[-0-9]+]}(%r{[sb]})p, %xmm1 # 16-byte Reload
```

```
; CHECK-NEXT: callq __subtf3@PLT
```

```
; CHECK-NEXT: testl %ebx, %ebx
```

```
; CHECK-NEXT: jg .LBB0_2
```

```
; CHECK-NEXT: # %bb.1:
```

```

; CHECK-NEXT: xorps %xmm0, %xmm0
; CHECK-NEXT: .LBB0_2:
; CHECK-NEXT: addq $32, %rsp
; CHECK-NEXT: .cfi_def_cfa_offset 16
; CHECK-NEXT: popq %rbx
; CHECK-NEXT: .cfi_def_cfa_offset 8
; CHECK-NEXT: retq
%cmp = fcmp ogt fp128 %a, %b
%sub = fsub fp128 %a, %b
%res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
ret fp128 %res
}

```

```

define fp128 @TestFabs(fp128 %a) {
; CHECK-LABEL: TestFabs:
; CHECK: # %bb.0:
; CHECK-NEXT: andps {{\?.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT: retq
%res = call fp128 @llvm.fabs.f128(fp128 %a)
ret fp128 %res
}

```

```

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestCopysign:
; CHECK: # %bb.0:
; CHECK-NEXT: andps {{\?.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1
; CHECK-NEXT: andps {{\?.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT: orps %xmm1, %xmm0
; CHECK-NEXT: retq
%res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
ret fp128 %res
}

```

```

define fp128 @TestFneg(fp128 %a) {
; CHECK-LABEL: TestFneg:
; CHECK: # %bb.0:
; CHECK-NEXT: pushq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 16
; CHECK-NEXT: movaps %xmm0, %xmm1
; CHECK-NEXT: callq __multf3@PLT
; CHECK-NEXT: xorps {{\?.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT: popq %rax
; CHECK-NEXT: .cfi_def_cfa_offset 8
; CHECK-NEXT: retq
%mul = fmul fp128 %a, %a
%res = fsub fp128 0xL00000000000000000800000000000000, %mul
ret fp128 %res
}

```

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```
; RUN: opt %s -inline -S | FileCheck %s
```

```
define internal void @innerSmall() "min-legal-vector-width"="128" {  
  ret void  
}
```

```
define internal void @innerLarge() "min-legal-vector-width"="512" {  
  ret void  
}
```

```
define internal void @innerNoAttribute() {  
  ret void  
}
```

```
; We should not add an attribute during inlining. No attribute means unknown.  
; Inlining doesn't change the fact that we don't know anything about this  
; function.
```

```
define void @outerNoAttribute() {  
  call void @innerLarge()  
  ret void  
}
```

```
define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {  
  call void @innerLarge()  
  ret void  
}
```

```
define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {  
  call void @innerSmall()  
  ret void  
}
```

```
; We should remove the attribute after inlining since the callee's  
; vector width requirements are unknown.
```

```
define void @outerAttribute() "min-legal-vector-width"="128" {  
  call void @innerNoAttribute()  
  ret void  
}
```

```

}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }

```

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```

; RUN: opt -consthoist -S -o - %s | FileCheck %s
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"
target triple = "thumbv6m-none--musleabi"

```

```

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*

```

```

; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8* %14, i8** @goo

```

```
@goo = global i8* undef
```

```

define void @foo_i8() {
entry:
%0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
%1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
%2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
%3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
%4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
store i8 %4, i8* inttoptr(i32 805873688 to i8*)
store i8 %3, i8* inttoptr(i32 805873719 to i8*)
store i8 %2, i8* inttoptr(i32 805873720 to i8*)
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}

```

```

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*

```

```

; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

```

```

define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void
}

```

```

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4

```

```
define void @foo_i32() {
entry:
%0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
%1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
%2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
%3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
%4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
%5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
ret void
}
```

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```
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --scrub-attributes
```

```
; RUN: opt -S -argpromotion < %s | FileCheck %s
```

```
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s
```

```
; Test that we only promote arguments when the caller/callee have compatible
```

```
; function attributes.
```

```
target triple = "x86_64-unknown-linux-gnu"
```

```
; This should promote
```

```
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {  
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512  
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])  
; CHECK-NEXT: bb:  
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]  
; CHECK-NEXT: ret void  
;  
bb:  
%tmp = load <8 x i64>, <8 x i64>* %arg1  
store <8 x i64> %tmp, <8 x i64>* %arg  
ret void  
}
```

```
define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {  
; CHECK-LABEL: define {{{^@+}}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512  
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])  
; CHECK-NEXT: bb:  
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32  
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*  
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)  
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]  
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])  
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32  
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2  
; CHECK-NEXT: ret void  
;  
bb:  
%tmp = alloca <8 x i64>, align 32  
%tmp2 = alloca <8 x i64>, align 32  
%tmp3 = bitcast <8 x i64>* %tmp to i8*
```

```

call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

; This should promote

```

define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

```

```

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void

```

```

}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {[^@]+}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

```

```

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {[^@]+}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

```

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {[^@]+}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512

```



```

; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@+}}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;

```

```

bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define {{{^@+}}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #2 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

```

```

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{{^@}+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x
i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

; This should promote

```

define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #3 {
; CHECK-LABEL: define {{{^@}+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

```

```

define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
; CHECK-LABEL: define {{{^@}+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

```

```

; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>*
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #4 {
; CHECK-LABEL: define {{{^@+}}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
%tmp = load <8 x i64>, <8 x i64>* %arg1
store <8 x i64> %tmp, <8 x i64>* %arg
ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
; CHECK-LABEL: define {{{^@+}}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>*
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

```

```

; CHECK-NEXT:  ret void
;
bb:
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}

```

; If the arguments are scalar, its ok to promote.

```

define internal i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %X, i32*
%Y) #2 {
; CHECK-LABEL: define
{[^[^@]+]}@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
; CHECK-NEXT:  [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT:  ret i32 [[C]]
;
%A = load i32, i32* %X
%B = load i32, i32* %Y
%C = add i32 %A, %B
ret i32 %C
}

```

```

define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
; CHECK-LABEL: define {[^[^@]+]}@scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (i32* [[B:%.*]])
; CHECK-NEXT:  [[A:%.*]] = alloca i32
; CHECK-NEXT:  store i32 1, i32* [[A]]
; CHECK-NEXT:  [[A_VAL:%.*]] = load i32, i32* [[A]]
; CHECK-NEXT:  [[B_VAL:%.*]] = load i32, i32* [[B]]
; CHECK-NEXT:  [[C:%.*]] = call i32
@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT:  ret i32 [[C]]
;
%A = alloca i32
store i32 1, i32* %A
%C = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %A, i32* %B)
ret i32 %C
}

```

; If the arguments are scalar, its ok to promote.

```

define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %X, i32*

```

```

%Y) #2 {
; CHECK-LABEL: define
{[{}@+]}@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
; CHECK-NEXT:  [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT:  ret i32 [[C]]
;
%A = load i32, i32* %X
%B = load i32, i32* %Y
%C = add i32 %A, %B
ret i32 %C
}

define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %B) #2 {
; CHECK-LABEL: define {[{}@+]}@scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (i32* [[B:%.*]])
; CHECK-NEXT:  [[A:%.*]] = alloca i32
; CHECK-NEXT:  store i32 1, i32* [[A]]
; CHECK-NEXT:  [[A_VAL:%.*]] = load i32, i32* [[A]]
; CHECK-NEXT:  [[B_VAL:%.*]] = load i32, i32* [[B]]
; CHECK-NEXT:  [[C:%.*]] = call i32
@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT:  ret i32 [[C]]
;
%A = alloca i32
store i32 1, i32* %A
%C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %A, i32* %B)
ret i32 %C
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512" "prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256" "prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }

```

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```
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -scalarize-masked-mem-intrin -S <%s | FileCheck %s
```

```
; Testing that masked scatters operating on scalable vectors that are  
; packed in SVE registers are not scalarized.
```

```
; CHECK-LABEL: @masked_scatter_nxv4i32(  
; CHECK: call void @llvm.masked.scatter.nxv4i32  
define void @masked_scatter_nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x i32*> %ptrs, <vscale x 4 x i1>  
%masks) {  
  call void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x i32*> %ptrs, i32 0, <vscale x 4 x  
i1> %masks)  
  ret void  
}
```

```
; Testing that masked scatters operating on scalable vectors of FP  
; data that is packed in SVE registers are not scalarized.
```

```
; CHECK-LABEL: @masked_scatter_nxv2f64(  
; CHECK: call void @llvm.masked.scatter.nxv2f64  
define void @masked_scatter_nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x double*> %ptrs, <vscale x 2 x  
i1> %masks) {  
  call void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x double*> %ptrs, i32 0,  
<vscale x 2 x i1> %masks)  
  ret void  
}
```

```
; Testing that masked scatters operating on scalable vectors of FP  
; data that is unpacked in SVE registers are not scalarized.
```

```
; CHECK-LABEL: @masked_scatter_nxv2f16(  
; CHECK: call void @llvm.masked.scatter.nxv2f16  
define void @masked_scatter_nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x half*> %ptrs, <vscale x 2 x i1>  
%masks) {  
  call void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x half*> %ptrs, i32 0, <vscale x 2  
x i1> %masks)  
  ret void  
}
```

```
; Testing that masked scatters operating on 64-bit fixed vectors are
; scalarized because NEON doesn't have support for masked scatter
; instructions.
```

```
; CHECK-LABEL: @masked_scatter_v2f32(
; CHECK-NOT: @llvm.masked.scatter.v2f32(
define void @masked_scatter_v2f32(<2 x float> %data, <2 x float*> %ptrs, <2 x i1> %masks) {
    call void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x float*> %ptrs, i32 0, <2 x i1> %masks)
    ret void
}
```

```
; Testing that masked scatters operating on 128-bit fixed vectors are
; scalarized because NEON doesn't have support for masked scatter
; instructions and because we are not targeting fixed width SVE.
```

```
; CHECK-LABEL: @masked_scatter_v4i32(
; CHECK-NOT: @llvm.masked.scatter.v4i32(
define void @masked_scatter_v4i32(<4 x i32> %data, <4 x i32*> %ptrs, <4 x i1> %masks) {
    call void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x i32*> %ptrs, i32 0, <4 x i1> %masks)
    ret void
}
```

```
declare void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x i32*> %ptrs, i32 %align,
<vscale x 4 x i1> %masks)
declare void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x double*> %ptrs, i32
%align, <vscale x 2 x i1> %masks)
declare void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x half*> %ptrs, i32 %align,
<vscale x 2 x i1> %masks)
declare void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x float*> %ptrs, i32 %align, <2 x i1> %masks)
declare void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x i32*> %ptrs, i32 %align, <4 x i1> %masks)
```

```
=====
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; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --include-generated-funcs

; RUN: opt -S -verify -iroutliner -ir-outlining-no-cost < %s | FileCheck %s

; This test checks that debug info is recognized as able to be extracted along with the other instructions, but is not included in the consolidated function.

```
define void @function1() !dbg !6 {
entry:
  %a = alloca i32, align 4, !dbg !17
  call void @llvm.dbg.value(metadata i32* %a, metadata !9, metadata !DIExpression()), !dbg !17
  %b = alloca i32, align 4, !dbg !18
  call void @llvm.dbg.value(metadata i32* %b, metadata !11, metadata !DIExpression()), !dbg !18
  %c = alloca i32, align 4, !dbg !19
```

```

call void @llvm.dbg.value(metadata i32* %c, metadata !12, metadata !DIExpression()), !dbg !19
store i32 2, i32* %a, align 4, !dbg !20
store i32 3, i32* %b, align 4, !dbg !21
store i32 4, i32* %c, align 4, !dbg !22
%al = load i32, i32* %a, align 4, !dbg !23
call void @llvm.dbg.value(metadata i32 %al, metadata !13, metadata !DIExpression()), !dbg !23
%bl = load i32, i32* %b, align 4, !dbg !24
call void @llvm.dbg.value(metadata i32 %bl, metadata !15, metadata !DIExpression()), !dbg !24
%cl = load i32, i32* %c, align 4, !dbg !25
call void @llvm.dbg.value(metadata i32 %cl, metadata !16, metadata !DIExpression()), !dbg !25
ret void, !dbg !26
}

```

```

define void @function2() !dbg !27 {
entry:
  %a = alloca i32, align 4, !dbg !35
  call void @llvm.dbg.value(metadata i32* %a, metadata !29, metadata !DIExpression()), !dbg !35
  %b = alloca i32, align 4, !dbg !36
  call void @llvm.dbg.value(metadata i32* %b, metadata !30, metadata !DIExpression()), !dbg !36
  %c = alloca i32, align 4, !dbg !37
  call void @llvm.dbg.value(metadata i32* %c, metadata !31, metadata !DIExpression()), !dbg !37
  store i32 2, i32* %a, align 4, !dbg !38
  store i32 3, i32* %b, align 4, !dbg !39
  store i32 4, i32* %c, align 4, !dbg !40
  %al = load i32, i32* %a, align 4, !dbg !41
  call void @llvm.dbg.value(metadata i32 %al, metadata !32, metadata !DIExpression()), !dbg !41
  %bl = load i32, i32* %b, align 4, !dbg !42
  call void @llvm.dbg.value(metadata i32 %bl, metadata !33, metadata !DIExpression()), !dbg !42
  %cl = load i32, i32* %c, align 4, !dbg !43
  call void @llvm.dbg.value(metadata i32 %cl, metadata !34, metadata !DIExpression()), !dbg !43
  ret void, !dbg !44
}

```

```

; Function Attrs: nounwind readnone speculatable willreturn
declare void @llvm.dbg.value(metadata, metadata, metadata) #0

```

```

attributes #0 = { nounwind readnone speculatable willreturn }

```

```

!llvm.dbg.cu = !{!0}
!llvm.debugify = !{!3, !4}
!llvm.module.flags = !{!5}

```

```

!0 = distinct !DICompileUnit(language: DW_LANG_C, file: !1, producer: "debugify", isOptimized: true,
runtimeVersion: 0, emissionKind: FullDebug, enums: !2)

```

```

!1 = !DIFile(filename: "legal-debug.ll", directory: "")

```

```

!2 = !{}

```

```

!3 = !{i32 20}

```

```

!4 = !{i32 12}
!5 = !{i32 2, !"Debug Info Version", i32 3}
!6 = distinct !DISubprogram(name: "function1", linkageName: "function1", scope: null, file: !1, line: 1, type: !7,
scopeLine: 1, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !8)
!7 = !DISubroutineType(types: !2)
!8 = !{!9, !11, !12, !13, !15, !16}
!9 = !DILocalVariable(name: "1", scope: !6, file: !1, line: 1, type: !10)
!10 = !DIBasicType(name: "ty64", size: 64, encoding: DW_ATE_unsigned)
!11 = !DILocalVariable(name: "2", scope: !6, file: !1, line: 2, type: !10)
!12 = !DILocalVariable(name: "3", scope: !6, file: !1, line: 3, type: !10)
!13 = !DILocalVariable(name: "4", scope: !6, file: !1, line: 7, type: !14)
!14 = !DIBasicType(name: "ty32", size: 32, encoding: DW_ATE_unsigned)
!15 = !DILocalVariable(name: "5", scope: !6, file: !1, line: 8, type: !14)
!16 = !DILocalVariable(name: "6", scope: !6, file: !1, line: 9, type: !14)
!17 = !DILocation(line: 1, column: 1, scope: !6)
!18 = !DILocation(line: 2, column: 1, scope: !6)
!19 = !DILocation(line: 3, column: 1, scope: !6)
!20 = !DILocation(line: 4, column: 1, scope: !6)
!21 = !DILocation(line: 5, column: 1, scope: !6)
!22 = !DILocation(line: 6, column: 1, scope: !6)
!23 = !DILocation(line: 7, column: 1, scope: !6)
!24 = !DILocation(line: 8, column: 1, scope: !6)
!25 = !DILocation(line: 9, column: 1, scope: !6)
!26 = !DILocation(line: 10, column: 1, scope: !6)
!27 = distinct !DISubprogram(name: "function2", linkageName: "function2", scope: null, file: !1, line: 11, type: !7,
scopeLine: 11, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !28)
!28 = !{!29, !30, !31, !32, !33, !34}
!29 = !DILocalVariable(name: "7", scope: !27, file: !1, line: 11, type: !10)
!30 = !DILocalVariable(name: "8", scope: !27, file: !1, line: 12, type: !10)
!31 = !DILocalVariable(name: "9", scope: !27, file: !1, line: 13, type: !10)
!32 = !DILocalVariable(name: "10", scope: !27, file: !1, line: 17, type: !14)
!33 = !DILocalVariable(name: "11", scope: !27, file: !1, line: 18, type: !14)
!34 = !DILocalVariable(name: "12", scope: !27, file: !1, line: 19, type: !14)
!35 = !DILocation(line: 11, column: 1, scope: !27)
!36 = !DILocation(line: 12, column: 1, scope: !27)
!37 = !DILocation(line: 13, column: 1, scope: !27)
!38 = !DILocation(line: 14, column: 1, scope: !27)
!39 = !DILocation(line: 15, column: 1, scope: !27)
!40 = !DILocation(line: 16, column: 1, scope: !27)
!41 = !DILocation(line: 17, column: 1, scope: !27)
!42 = !DILocation(line: 18, column: 1, scope: !27)
!43 = !DILocation(line: 19, column: 1, scope: !27)
!44 = !DILocation(line: 20, column: 1, scope: !27)
; CHECK-LABEL: @function1(
; CHECK-NEXT: entry:
; CHECK-NEXT:  [[A:%.*]] = alloca i32, align 4, !dbg [[DBG17:![0-9]+]]
; CHECK-NEXT:  call void @llvm.dbg.value(metadata i32* [[A]], metadata [[META9:![0-9]+]], metadata
!DIExpression(), !dbg [[DBG17]]

```

```

; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4, !dbg [[DBG18:[0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[B]], metadata [[META11:[0-9]+]], metadata
!DIExpression(), !dbg [[DBG18]]
; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4, !dbg [[DBG19:[0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[C]], metadata [[META12:[0-9]+]], metadata
!DIExpression(), !dbg [[DBG19]]
; CHECK-NEXT: call void @outlined_ir_func_0(i32* [[A]], i32* [[B]], i32* [[C]], !dbg [[DBG20:[0-9]+]]
; CHECK-NEXT: ret void, !dbg [[DBG21:[0-9]+]]
;
;
; CHECK-LABEL: @function2(
; CHECK-NEXT: entry:
; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4, !dbg [[DBG30:[0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[A]], metadata [[META24:[0-9]+]], metadata
!DIExpression(), !dbg [[DBG30]]
; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4, !dbg [[DBG31:[0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[B]], metadata [[META25:[0-9]+]], metadata
!DIExpression(), !dbg [[DBG31]]
; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4, !dbg [[DBG32:[0-9]+]]
; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[C]], metadata [[META26:[0-9]+]], metadata
!DIExpression(), !dbg [[DBG32]]
; CHECK-NEXT: call void @outlined_ir_func_0(i32* [[A]], i32* [[B]], i32* [[C]], !dbg [[DBG33:[0-9]+]]
; CHECK-NEXT: ret void, !dbg [[DBG34:[0-9]+]]
;
;
; CHECK: @outlined_ir_func_0(i32* [[TMP0:%.*]], i32* [[TMP1:%.*]], i32* [[TMP2:%.*]])
; CHECK: entry_to_outline:
; CHECK-NEXT: store i32 2, i32* [[TMP0]], align 4
; CHECK-NEXT: store i32 3, i32* [[TMP1]], align 4
; CHECK-NEXT: store i32 4, i32* [[TMP2]], align 4
; CHECK-NEXT: [[AL:%.*]] = load i32, i32* [[TMP0]], align 4
; CHECK-NEXT: [[BL:%.*]] = load i32, i32* [[TMP1]], align 4
; CHECK-NEXT: [[CL:%.*]] = load i32, i32* [[TMP2]], align 4
; CHECK-NEXT: br label [[ENTRY_AFTER_OUTLINE_EXITSTUB:%.*]]
;

```

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```
add_llvm_library(llvmPluginObjectContainerBSDArchive PLUGIN
ObjectContainerBSDArchive.cpp
```

```
LINK_LIBS
```

```
  llvmCore
```

```
  llvmHost
```

```
  llvmSymbol
```

```
LINK_COMPONENTS
```

```
  Support
```

```
)
```

```
; RUN: llc -march=hexagon -hexagon-hvx-widen=32 < %s | FileCheck %s
```

```
; Truncating a type-to-be-widened to a legal type (v8i8).
```

```
; Check that this compiles successfully.
```

```
; CHECK-LABEL: f0:
```

```
; CHECK: dealloc_return
```

```
target datalayout = "e-m:e-p:32:32:32-a:0-n16:32-i64:64:64-i32:32:32-i16:16:16-i1:8:8-f32:32:32-f64:64:64-v32:32:32-v64:64:64-v512:512:512-v1024:1024:1024-v2048:2048:2048"
```

```
target triple = "hexagon"
```

```
define dlllexport void @f0(i8* %a0) local_unnamed_addr #0 {
```

```
b0:
```

```
  %v0 = load i8, i8* undef, align 1
```

```
  %v1 = zext i8 %v0 to i16
```

```
  %v2 = add i16 0, %v1
```

```
  %v3 = icmp sgt i16 %v2, 1
```

```
  %v4 = select i1 %v3, i16 %v2, i16 1
```

```
  %v5 = udiv i16 -32768, %v4
```

```
  %v6 = zext i16 %v5 to i32
```

```
  %v7 = insertelement <8 x i32> undef, i32 %v6, i32 0
```

```
  %v8 = shufflevector <8 x i32> %v7, <8 x i32> undef, <8 x i32> zeroinitializer
```

```
  %v9 = load <8 x i16>, <8 x i16>* undef, align 2
```

```
  %v10 = sext <8 x i16> %v9 to <8 x i32>
```

```
  %v11 = mul nsw <8 x i32> %v8, %v10
```

```
  %v12 = add nsw <8 x i32> %v11, <i32 16384, i32 16384, i32 16384, i32 16384, i32 16384, i32 16384, i32 16384, i32 16384,
```

```

i32 16384>
%v13 = lshr <8 x i32> %v12, <i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15>
%v14 = trunc <8 x i32> %v13 to <8 x i8>
%v15 = getelementptr inbounds i8, i8* %a0, i32 undef
%v16 = bitcast i8* %v15 to <8 x i8>*
store <8 x i8> %v14, <8 x i8>* %v16, align 1
ret void
}

```

```

attributes #0 = { "target-features"="+hvx,+hvx-length128b" }
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

```

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

```
target triple = "hexagon"
```

```

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

```

```

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
br i1 undef, label %while.end, label %while.body.lr.ph

```

```

while.body.lr.ph:                ; preds = %entry
br label %while.body

```

```

while.body:                        ; preds = %exit.2, %while.body.lr.ph
%lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
switch i32 undef, label %exit [
  i32 1, label %sw.bb.i
  i32 2, label %sw.bb3.i
]

```

```

sw.bb.i:                            ; preds = %while.body
unreachable

```

```

sw.bb3.i:                            ; preds = %while.body
unreachable

```

```

exit:                                ; preds = %while.body
switch i32 undef, label %exit.2 [
  i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
]

```

```

sw.bb.i17:                                ; preds = %.exit
%0 = bitcast %struct.0* %lshr.iv to i32*
%1 = load i32, i32* %0, align 4
unreachable

sw.bb3.i20:                                ; preds = %exit
%2 = bitcast %struct.0* %lshr.iv to i8**
%3 = load i8*, i8** %2, align 4
unreachable

exit.2:                                    ; preds = %exit
%cgep22 = getelementptr %struct.0, %struct.0* %lshr.iv, i32 1
br label %while.body

while.end:                                  ; preds = %entry
ret void
}

```

```

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
LLVM System Interface Library

```

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See <https://llvm.org/LICENSE.txt> for license information.

SPDX-License-Identifier: Apache-2.0 WITH LLVM-exception

; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py

; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=VEC256,AVX

; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,AVX512VL256

; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,-prefer-256-bit | FileCheck %s --check-prefixes=AVX512VL512

; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -

mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,SKX256

; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -

mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=SKX512

```

define void @zext256() "min-legal-vector-width"="256" {

```

```

; AVX-LABEL: 'zext256'

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32> undef to <8 x i64>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

```

```

;

```

```

; AVX512VL256-LABEL: 'zext256'

```

```

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext256'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'zext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x

```

```

i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'zext512'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext512'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'

```

```

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'zext512'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = zext <8 x i16> undef to <8 x i64>
%B = zext <8 x i32> undef to <8 x i64>
%C = zext <16 x i8> undef to <16 x i32>
%D = zext <16 x i16> undef to <16 x i32>
%E = zext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext256() "min-legal-vector-width"="256" {
; AVX-LABEL: 'sext256'
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'sext256'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to
<8 x i64>

```

```

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext256'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x

```



```

i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'sext512'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext512'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8
x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to
<16 x i32>

```

```

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext512'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = sext <8 x i8> undef to <8 x i64>
%B = sext <8 x i16> undef to <8 x i64>
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'trunc256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x
i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %B = trunc <8 x i64> undef to <8 x

```

```

i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %C = trunc <8 x i64> undef to <8 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = trunc <16 x i32> undef to <16 x
i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = trunc <16 x i32> undef to <16 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = trunc <32 x i16> undef to <32 x
i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'trunc256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to
<8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to
<8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef
to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to
<16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to
<32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'trunc256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %F = trunc <32 x i16> undef to <32 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
%A = trunc <8 x i64> undef to <8 x i32>
%B = trunc <8 x i64> undef to <8 x i16>
%C = trunc <8 x i64> undef to <8 x i8>
%D = trunc <16 x i32> undef to <16 x i16>
%E = trunc <16 x i32> undef to <16 x i8>
%F = trunc <32 x i16> undef to <32 x i8>
ret void

```

```

}

define i32 @zext256_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'zext256_vXi1'
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'zext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

```

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 50 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'zext256_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = zext <4 x i1> undef

```

to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef
to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1>
undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1>
undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8 = zext <2 x i1> undef to
<2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to
<4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef
to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef
to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1>
undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'zext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to
<16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to
<16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = zext <32 x i1> undef to
<32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x
i8>

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; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16
x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32
x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = zext <64 x i1> undef to <64
x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'zext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x
i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x
i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to
<16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x
i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to
<16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = zext <32 x i1> undef to
<32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x
i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16
x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32
x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64

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x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%V2i64 = zext <2 x i1> undef to <2 x i64>
%V4i64 = zext <4 x i1> undef to <4 x i64>
%V8i64 = zext <8 x i1> undef to <8 x i64>

%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>

%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i16 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>

%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @sext256_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'sext256_vXi1'
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x
i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x
i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = sext <8 x i1> undef to <8 x
i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = sext <16 x i1> undef to <16 x
i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x

```



```

i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = sext <4 x i1> undef to <4 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = sext <8 x i1> undef to <8 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x
i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = sext <16 x i1> undef to <16 x
i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x
i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x
i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'sext256_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef
to <2 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef
to <4 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef
to <8 x i64>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef
to <2 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef
to <4 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef
to <8 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1>
undef to <16 x i32>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = sext <2 x i1> undef
to <2 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = sext <4 x i1> undef
to <4 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = sext <8 x i1> undef
to <8 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i16 = sext <16 x i1>
undef to <16 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V32i16 = sext <32 x i1>

```

```

undef to <32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to
<2 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i8 = sext <4 x i1> undef to
<4 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to
<8 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i8 = sext <16 x i1>
undef to <16 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1>
undef to <32 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1>
undef to <64 x i8>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'sext256_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef
to <2 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef
to <4 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef
to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef
to <2 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef
to <4 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef
to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1>
undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = sext <2 x i1> undef
to <2 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = sext <4 x i1> undef
to <4 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = sext <8 x i1> undef
to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1>
undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = sext <32 x i1>
undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = sext <2 x i1> undef to
<2 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = sext <4 x i1> undef to

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<4 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to
<8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = sext <16 x i1> undef
to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef
to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1>
undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'sext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x
i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x
i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to
<16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x
i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to
<16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to
<32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x
i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16
x i8>

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; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'sext256_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

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;
%I64 = sext i1 undef to i64
%V2i64 = sext <2 x i1> undef to <2 x i64>
%V4i64 = sext <4 x i1> undef to <4 x i64>
%V8i64 = sext <8 x i1> undef to <8 x i64>

%I32 = sext i1 undef to i32
%V2i32 = sext <2 x i1> undef to <2 x i32>
%V4i32 = sext <4 x i1> undef to <4 x i32>
%V8i32 = sext <8 x i1> undef to <8 x i32>
%V16i32 = sext <16 x i1> undef to <16 x i32>

%I16 = sext i1 undef to i16
%V2i16 = sext <2 x i1> undef to <2 x i16>
%V4i16 = sext <4 x i1> undef to <4 x i16>
%V8i16 = sext <8 x i1> undef to <8 x i16>
%V16i16 = sext <16 x i1> undef to <16 x i16>
%V32i16 = sext <32 x i1> undef to <32 x i16>

%I8 = sext i1 undef to i8
%V2i8 = sext <2 x i1> undef to <2 x i8>
%V4i8 = sext <4 x i1> undef to <4 x i8>
%V8i8 = sext <8 x i1> undef to <8 x i8>
%V16i8 = sext <16 x i1> undef to <16 x i8>
%V32i8 = sext <32 x i1> undef to <32 x i8>
%V64i8 = sext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'trunc_vXi1'
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to
<16 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to
<32 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 46 for instruction: %V64i64 = trunc <64 x i64> undef to
<64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x
i1>

```

```

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i32 = trunc <16 x i32> undef to <16
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i32 = trunc <32 x i32> undef to
<32 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i32 = trunc <64 x i32> undef to
<64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = trunc <16 x i16> undef to <16
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = trunc <32 x i16> undef to <32
x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 18 for instruction: %V64i16 = trunc <64 x i16> undef to
<64 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x
i1>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL256-LABEL: 'trunc_vXi1'
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64>
undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64>
undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64>
undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32>
undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32>
undef to <4 x i1>

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; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32>
undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V32i32 = trunc <32 x i32>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V64i32 = trunc <64 x i32>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16>
undef to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16>
undef to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16>
undef to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i16 = trunc <16 x i16>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V32i16 = trunc <32 x i16>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V64i16 = trunc <64 x i16>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef
to <2 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef
to <4 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef
to <8 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i8 = trunc <16 x i8>
undef to <16 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i8 = trunc <32 x i8>
undef to <32 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i8 = trunc <64 x i8>
undef to <64 x i1>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; AVX512VL512-LABEL: 'trunc_vXi1'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64>
undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64>
undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64>
undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64>
undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32>

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undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32>
undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32>
undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32>
undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i32 = trunc <32 x i32>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16>
undef to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16>
undef to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16>
undef to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = trunc <16 x i16>
undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = trunc <32 x i16>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 14 for instruction: %V64i16 = trunc <64 x i16>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef
to <2 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef
to <4 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef
to <8 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = trunc <16 x i8>
undef to <16 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = trunc <32 x i8>
undef to <32 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = trunc <64 x i8>
undef to <64 x i1>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'trunc_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to
<32 x i1>

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; SKX256-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V32i32 = trunc <32 x i32> undef to
<32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V64i32 = trunc <64 x i32> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8
x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = trunc <32 x i16> undef to
<32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i16 = trunc <64 x i16> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x
i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x
i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x
i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to
<16 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to
<32 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = trunc <64 x i8> undef to
<64 x i1>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'trunc_vXi1'
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to

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<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i32 = trunc <32 x i32> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i32 = trunc <64 x i32> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8
x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = trunc <32 x i16> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i16 = trunc <64 x i16> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x
i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x
i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x
i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to
<16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to
<32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = trunc <64 x i8> undef to
<64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
%V2i64 = trunc <2 x i64> undef to <2 x i1>
%V4i64 = trunc <4 x i64> undef to <4 x i1>
%V8i64 = trunc <8 x i64> undef to <8 x i1>
%V16i64 = trunc <16 x i64> undef to <16 x i1>
%V32i64 = trunc <32 x i64> undef to <32 x i1>

```

%V64i64 = trunc <64 x i64> undef to <64 x i1>

%V2i32 = trunc <2 x i32> undef to <2 x i1>

%V4i32 = trunc <4 x i32> undef to <4 x i1>

%V8i32 = trunc <8 x i32> undef to <8 x i1>

%V16i32 = trunc <16 x i32> undef to <16 x i1>

%V32i32 = trunc <32 x i32> undef to <32 x i1>

%V64i32 = trunc <64 x i32> undef to <64 x i1>

%V2i16 = trunc <2 x i16> undef to <2 x i1>

%V4i16 = trunc <4 x i16> undef to <4 x i1>

%V8i16 = trunc <8 x i16> undef to <8 x i1>

%V16i16 = trunc <16 x i16> undef to <16 x i1>

%V32i16 = trunc <32 x i16> undef to <32 x i1>

%V64i16 = trunc <64 x i16> undef to <64 x i1>

%V2i8 = trunc <2 x i8> undef to <2 x i1>

%V4i8 = trunc <4 x i8> undef to <4 x i1>

%V8i8 = trunc <8 x i8> undef to <8 x i1>

%V16i8 = trunc <16 x i8> undef to <16 x i1>

%V32i8 = trunc <32 x i8> undef to <32 x i1>

%V64i8 = trunc <64 x i8> undef to <64 x i1>

ret i32 undef

}

; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py

; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {

; CHECK-LABEL: test_sitofp_fixed:

; CHECK: ; %bb.0:

; CHECK-NEXT: sshll.2d v4, v2, #0

; CHECK-NEXT: sshll.2d v16, v1, #0

; CHECK-NEXT: sshll.2d v5, v0, #0

; CHECK-NEXT: sshll.2d v6, v1, #0

; CHECK-NEXT: sshll.2d v7, v3, #0

; CHECK-NEXT: sshll.2d v0, v0, #0

; CHECK-NEXT: sshll.2d v17, v2, #0

; CHECK-NEXT: sshll.2d v18, v3, #0

; CHECK-NEXT: scvtf.2d v1, v5, #6

; CHECK-NEXT: scvtf.2d v3, v6, #6

; CHECK-NEXT: scvtf.2d v2, v16, #6

; CHECK-NEXT: scvtf.2d v5, v4, #6

; CHECK-NEXT: scvtf.2d v0, v0, #6

; CHECK-NEXT: scvtf.2d v7, v7, #6

; CHECK-NEXT: scvtf.2d v4, v17, #6

; CHECK-NEXT: scvtf.2d v6, v18, #6

; CHECK-NEXT: ret

```

%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0>
ret <16 x double> %res
}

```

; This one is small enough to satisfy isSimple, but still illegally large.

```

define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:
; CHECK:      ; %bb.0:
; CHECK-NEXT:  scvtf.2d v0, v0, #6
; CHECK-NEXT:  scvtf.2d v1, v1, #6
; CHECK-NEXT:  ret

```

```

%flt = sitofp <4 x i64> %in to <4 x double>
%res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
ret <4 x double> %res
}

```

=====
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```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s
--check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi |
FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for
vpmaddwd+vpadd
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-
prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --
check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --
check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-
prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-client | FileCheck %s --
check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-server | FileCheck %s --
check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=tigerlake | FileCheck %s --check-
prefixes=CHECK,CHECK-VBMI
```

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

```
define dso_local void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-
width"="256" {
; CHECK-LABEL: add256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpadd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vpadd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
```



```

%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define dso_local void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-
legal-vector-width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:  vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:  vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%A = load <32 x i16>, <32 x i16>* %APtr
%B = load <32 x i16>, <32 x i16>* %BPtr
%a = sext <32 x i16> %A to <32 x i32>
%b = sext <32 x i16> %B to <32 x i32>
%m = mul nsw <32 x i32> %a, %b
%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
%ret = add <16 x i32> %odd, %even
store <16 x i32> %ret, <16 x i32>* %CPtr
ret void
}

```

```

define dso_local void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:  vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x

```

```

%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define dso_local void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-
vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <64 x i8>, <64 x i8>* %xptr
%y = load <64 x i8>, <64 x i8>* %yptr
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}

```

```

define dso_local i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-
vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB8_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vpmovsxbw 16(%rdi,%rcx), %ymm3
; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-NEXT: vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-NEXT: vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT: vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %ymm3
; CHECK-NEXT: vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT: vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT: addq $32, %rcx
; CHECK-NEXT: cmpq %rcx, %rax
; CHECK-NEXT: jne .LBB8_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm1

```

```

; CHECK-NEXT: vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {.*#+} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpshufd {.*#+} xmm1 = xmm0[1,1,1,1]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq

```

entry:

```
%3 = zext i32 %2 to i64
```

```
br label %vector.body
```

vector.body:

```

%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

```

middle.block:

```

%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15

```

```

%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}

```

```

define dso_local i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-
vector-width"="512" {

```

```

; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT:  movl %edx, %eax
; CHECK-NEXT:  vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:  xorl %ecx, %ecx
; CHECK-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:  .p2align 4, 0x90
; CHECK-NEXT: .LBB9_1: # %vector.body
; CHECK-NEXT:  # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:  vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT:  vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT:  vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:  vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:  addq $32, %rcx
; CHECK-NEXT:  cmpq %rcx, %rax
; CHECK-NEXT:  jne .LBB9_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:  vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:  vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:  vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-NEXT:  vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:  vmovd %xmm0, %eax
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
entry:
%3 = zext i32 %2 to i64
br label %vector.body

```


vector.body:

```
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body
```

middle.block:

```
%rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
%bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
%rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
%rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
%rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
%rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
%13 = extractelement <32 x i32> %bin.rdx20, i32 0
ret i32 %13
}
```

@a = dso_local global [1024 x i8] zeroinitializer, align 16

@b = dso_local global [1024 x i8] zeroinitializer, align 16

```
define dso_local i32 @sad_16i8_256() "min-legal-vector-width"="256" {
```

```
; CHECK-LABEL: sad_16i8_256:
```

```
; CHECK:      # %bb.0: # %entry
```

```
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
```

```
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
```

```
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
```

```
; CHECK-NEXT: .p2align 4, 0x90
```

```
; CHECK-NEXT: .LBB10_1: # %vector.body
```

```
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
```

```
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm2
```

```
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
```

```
; CHECK-NEXT: vpadd %ymm1, %ymm2, %ymm1
```

```
; CHECK-NEXT: addq $4, %rax
```

```
; CHECK-NEXT: jne .LBB10_1
```

```
; CHECK-NEXT: # %bb.2: # %middle.block
```

```
; CHECK-NEXT: vpadd %ymm0, %ymm1, %ymm0
```

```
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vpsdshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vpsdshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
```

```
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
```

```
; CHECK-NEXT: vmovd %xmm0, %eax
```

```
; CHECK-NEXT: vzeroupper
```

```
; CHECK-NEXT: retq
```

```
entry:
```

```
br label %vector.body
```

```
vector.body:
```

```
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
```

```
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
```

```
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
```

```
%1 = bitcast i8* %0 to <16 x i8>*
```

```
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
```

```
%2 = zext <16 x i8> %wide.load to <16 x i32>
```

```
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
```

```
%4 = bitcast i8* %3 to <16 x i8>*
```

```
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
```

```
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
```

```
%6 = sub nsw <16 x i32> %2, %5
```

```
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
```

```
%8 = sub nsw <16 x i32> zeroinitializer, %6
```

```
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
```

```
%10 = add nsw <16 x i32> %9, %vec.phi
```

```

%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

```

middle.block:

```

%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32
13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

```

```

define dso_local i32 @sad_16i8_512() "min-legal-vector-width"="512" {

```

```

; CHECK-LABEL: sad_16i8_512:
; CHECK:      # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB11_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-NEXT: vpadd %zmm0, %zmm1, %zmm0
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB11_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT: vpadd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpsltd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vpsltd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-NEXT: vpadd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper

```

```

; CHECK-NEXT:    retq
entry:
br label %vector.body

vector.body:
%index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
%vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %10, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define dso_local void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:    # %bb.0:

```

```

; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvt dq2ps %ymm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm1
; CHECK-NEXT: vcvt dq2ps %ymm1, %ymm1
; CHECK-NEXT: vmovaps %ymm1, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

```

```

define dso_local void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vcvt dq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

```

```

define dso_local void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vcvt dq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvt dq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vcvt dq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvt dq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)

```

```

; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define dso_local void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  vpmovm2d %k0, %zmm0
; CHECK-NEXT:  vcvt dq2pd %ymm0, %zmm1
; CHECK-NEXT:  vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:  vcvt dq2pd %ymm0, %zmm0
; CHECK-NEXT:  vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:  vmovaps %zmm1, (%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define dso_local void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vpmovw2m %ymm0, %k0
; CHECK-NEXT:  kshiftrw $8, %k0, %k1
; CHECK-NEXT:  vpmovm2d %k1, %ymm0
; CHECK-NEXT:  vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:  vcvt dq2ps %ymm0, %ymm0
; CHECK-NEXT:  vpmovm2d %k0, %ymm1
; CHECK-NEXT:  vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT:  vcvt dq2ps %ymm1, %ymm1
; CHECK-NEXT:  vmovaps %ymm1, (%rdi)
; CHECK-NEXT:  vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define dso_local void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {

```

```

; CHECK-LABEL: ubto16f32_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT: vcvt dq2ps %zmm0, %zmm0
; CHECK-NEXT: vmovaps %zmm0, (%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}

define dso_local void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: kshiftrw $8, %k0, %k1
; CHECK-NEXT: vpmovm2d %k1, %ymm0
; CHECK-NEXT: vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT: vcvt dq2pd %xmm0, %ymm1
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT: vcvt dq2pd %xmm0, %ymm0
; CHECK-NEXT: vpmovm2d %k0, %ymm2
; CHECK-NEXT: vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT: vcvt dq2pd %xmm2, %ymm3
; CHECK-NEXT: vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT: vcvt dq2pd %xmm2, %ymm2
; CHECK-NEXT: vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT: vmovaps %ymm3, (%rdi)
; CHECK-NEXT: vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT: vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define dso_local void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:      # %bb.0:
; CHECK-NEXT: vpmovw2m %ymm0, %k0
; CHECK-NEXT: vpmovm2d %k0, %zmm0
; CHECK-NEXT: vpsrld $31, %zmm0, %zmm0

```

```

; CHECK-NEXT:   vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:   vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:   vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:   vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:   vmovaps %zmm1, (%rdi)
; CHECK-NEXT:   vzeroupper
; CHECK-NEXT:   retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:   vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:   vpmovd2m %ymm1, %k0
; CHECK-NEXT:   vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:   vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:   vpmovd2m %ymm1, %k1
; CHECK-NEXT:   kunpckbw %k0, %k1, %k1
; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:   retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:   vpslld $31, %zmm1, %zmm1
; CHECK-NEXT:   vpmovd2m %zmm1, %k1
; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:   retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-

```



```

width="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k0
; CHECK-NEXT:  vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovd2m %ymm1, %k1
; CHECK-NEXT:  kunpckbw %k0, %k1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:  vpmovd2m %zmm1, %k1
; CHECK-NEXT:  vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:  retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptosi <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define dso_local void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width="256" {
; CHECK-AVX512-LABEL: mul256:
; CHECK-AVX512:    # %bb.0:
; CHECK-AVX512-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-AVX512-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-AVX512-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-AVX512-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} %ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpmullw %ymm4, %ymm5, %ymm4
; CHECK-AVX512-NEXT:  vmovdqa {{.*#+}} %ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} %ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} %ymm1 =

```

```

ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpmullw %ymm3, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm3 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpmullw %ymm3, %ymm4, %ymm3
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm3, %ymm3
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT:  vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT:  vzeroupper
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI:      # %bb.0:
; CHECK-VBMI-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT:  vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT:  vmovdqa 32(%rsi), %ymm3
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:  vpmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT:  vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT:  vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm4 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]

```



```

; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm2 =
zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:  vpmullw %zmm2, %zmm3, %zmm2
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT:  vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT:  vmovdqa64 {{.*#+}} zmm1 =
[0,2,4,6,8,10,12,14,64,66,68,70,72,74,76,78,16,18,20,22,24,26,28,30,80,82,84,86,88,90,92,94,32,34,36,38,40,42,44,
46,96,98,100,102,104,106,108,110,48,50,52,54,56,58,60,62,112,114,116,118,120,122,124,126]
; CHECK-VBMI-NEXT:  vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT:  vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT:  vzeroupper
; CHECK-VBMI-NEXT:  retq
%d = load <64 x i8>, <64 x i8>* %a
%e = load <64 x i8>, <64 x i8>* %b
%f = mul <64 x i8> %d, %e
store <64 x i8> %f, <64 x i8>* %c
ret void
}

```

; This threw an assertion at one point.

```

define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-
width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT:  vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT:  retq
%mask = icmp eq <4 x i32> %trigger, zeroinitializer
%res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32>
%dst)
ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)

```

```

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
; CHECK:      # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1

```

```

; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqd %ymm0, %xmm0
; CHECK-NEXT: vpmovqd %ymm1, %xmm1
; CHECK-NEXT: vinserti128 $1, %xmm1, %ymm0, %ymm0
; CHECK-NEXT: vpmovqd %ymm2, %xmm1
; CHECK-NEXT: vpmovqd %ymm3, %xmm2
; CHECK-NEXT: vinserti128 $1, %xmm2, %ymm1, %ymm1
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i32>
ret <16 x i32> %b
}

```

```

define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i8:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqb %ymm3, %xmm3
; CHECK-NEXT: vpmovqb %ymm2, %xmm2
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
; CHECK-NEXT: vpmovqb %ymm1, %xmm1
; CHECK-NEXT: vpmovqb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm2[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i64>, <16 x i64>* %x
%b = trunc <16 x i64> %a to <16 x i8>
ret <16 x i8> %b
}

```

```

define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK:    # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmovdb %ymm1, %xmm1
; CHECK-NEXT: vpmovdb %ymm0, %xmm0
; CHECK-NEXT: vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %x
%b = trunc <16 x i32> %a to <16 x i8>
ret <16 x i8> %b
}

```

```

}

define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqb %ymm1, %xmm1
; CHECK-NEXT:  vpmovqb %ymm0, %xmm0
; CHECK-NEXT:  vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i8>
ret <8 x i8> %b
}

```

```

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i16:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:  vpmovqw %ymm1, %xmm1
; CHECK-NEXT:  vpmovqw %ymm0, %xmm0
; CHECK-NEXT:  vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = trunc <8 x i64> %a to <8 x i16>
ret <8 x i16> %b
}

```

```

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vpsrlq $48, 32(%rdi), %ymm0
; CHECK-NEXT:  vpsrlq $48, (%rdi), %ymm1
; CHECK-NEXT:  vpackusdw %ymm0, %ymm1, %ymm0
; CHECK-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:  retq
%a = load <8 x i64>, <8 x i64>* %x
%b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
%c = trunc <8 x i64> %b to <8 x i32>
ret <8 x i32> %c
}

```

```

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:

```



```

; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm2 =
xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm3 =
xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm1 =
xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero
; CHECK-NEXT: vpmovxbq {{.*#+}} ymm0 =
xmm0[0],zero,zero,zero,zero,zero,zero,zero,xmm0[1],zero,zero,zero,zero,zero,zero,zero,xmm0[2],zero,zero,zero,zer
o,zero,zero,zero,xmm0[3],zero,zero,zero,zero,zero,zero,zero
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = zext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

```

```

define dso_local void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-
width"="256" {

```

```

; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovsxbw %xmm0, %ymm1
; CHECK-NEXT: vpshufd {{.*#+}} xmm2 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovswwq %xmm2, %ymm2
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovswwq %xmm3, %ymm3
; CHECK-NEXT: vpmovswwq %xmm1, %ymm1
; CHECK-NEXT: vpmovsxbq %xmm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = sext <16 x i8> %x to <16 x i64>
store <16 x i64> %a, <16 x i64>* %y
ret void
}

```

```

define dso_local void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256" {

```

```

; CHECK-LABEL: vselect_split_v8i16_setcc:

```

```

; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i16> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

define dso_local void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqd %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %p
%y = load <8 x i64>, <8 x i64>* %q
%a = icmp eq <8 x i32> %s, %t
%b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
store <8 x i64> %b, <8 x i64>* %r
ret void
}

define dso_local void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q,
<16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK:      # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqb %xmm1, %xmm0, %k1

```

```

; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i8> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

define dso_local void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>*
%q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT: kshiftrw $8, %k1, %k2
; CHECK-NEXT: vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT: vmovdqa %ymm2, (%rdx)
; CHECK-NEXT: vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <16 x i32>, <16 x i32>* %p
%y = load <16 x i32>, <16 x i32>* %q
%a = icmp eq <16 x i16> %s, %t
%b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
store <16 x i32> %b, <16 x i32>* %r
ret void
}

define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpermq { {. *#+} } ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT: vpmovuswb %ymm0, %xmm0
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32

```

```

255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
ret <16 x i8> %f
}

define dso_local void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
; CHECK:    # %bb.0:
; CHECK-NEXT:  vmovdqa (%rdi), %ymm0
; CHECK-NEXT:  vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT:  vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:  vpmovuswb %ymm0, (%rsi)
; CHECK-NEXT:  vzeroupper
; CHECK-NEXT:  retq
%a = load <16 x i32>, <16 x i32>* %p
%b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
%d = icmp sgt <16 x i32> %c, zeroinitializer
%e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
%f = trunc <16 x i32> %e to <16 x i8>
store <16 x i8> %f, <16 x i8>* %q
ret void
}

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_argument_return:
; CHECK:    # %bb.0:
; CHECK-NEXT:  retq
ret <64 x i1> %x
}

define dso_local void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_shuffle:
; CHECK:    # %bb.0: # %entry
; CHECK-NEXT:  vmovdqa (%rdi), %ymm1
; CHECK-NEXT:  vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT:  vptestnmb %ymm1, %ymm1, %k0
; CHECK-NEXT:  kshiftrd $1, %k0, %k1
; CHECK-NEXT:  movq $-3, %rax
; CHECK-NEXT:  kmovq %rax, %k2
; CHECK-NEXT:  kandq %k2, %k1, %k1

```

```

; CHECK-NEXT: kshiftrlq $63, %k0, %k2
; CHECK-NEXT: kshiftrq $62, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-5, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $3, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $61, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-9, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $2, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $60, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-17, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $5, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $59, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-33, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $4, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $58, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $7, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $57, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-129, %rax
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $6, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $56, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1

```

```

; CHECK-NEXT: kshiftrd $9, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $55, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-513, %rax # imm = 0xFDFD
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $8, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $54, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $11, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $53, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $10, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $52, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $13, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $51, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $12, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $50, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $15, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $49, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT: kmovq %rax, %k2

```

```

; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $14, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $48, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-65537, %rax # imm = 0xFFFEFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $17, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $47, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-131073, %rax # imm = 0xFFFDFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $16, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $46, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-262145, %rax # imm = 0xFFFBFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $19, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $45, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-524289, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $18, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $44, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1048577, %rax # imm = 0xFFEFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $21, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $43, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-2097153, %rax # imm = 0xFFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $20, %k0, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $42, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-4194305, %rax # imm = 0xFFBFFFFFFF

```

```

; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $23, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $41, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-8388609, %rax # imm = 0xFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $22, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $40, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-16777217, %rax # imm = 0xFEFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $25, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $39, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-33554433, %rax # imm = 0xFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $24, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $38, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-67108865, %rax # imm = 0xFBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $27, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $37, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-134217729, %rax # imm = 0xF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $26, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $36, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $29, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $35, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1

```



```

; CHECK-NEXT: movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $28, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $34, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k1
; CHECK-NEXT: kshiftrd $31, %k0, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $33, %k2, %k2
; CHECK-NEXT: korq %k2, %k1, %k1
; CHECK-NEXT: movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k1, %k2
; CHECK-NEXT: vptestnmb %ymm0, %ymm0, %k1
; CHECK-NEXT: kshiftrd $30, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k0, %k0
; CHECK-NEXT: kshiftrq $32, %k0, %k0
; CHECK-NEXT: korq %k0, %k2, %k0
; CHECK-NEXT: movabsq $-4294967297, %rax # imm = 0xFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $1, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $31, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8589934593, %rax # imm = 0xFFFFFFFFDFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrlq $63, %k1, %k2
; CHECK-NEXT: kshiftrq $30, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17179869185, %rax # imm = 0xFFFFFFFFBFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $3, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $29, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-34359738369, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $2, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $28, %k2, %k2

```

```

; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-68719476737, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $5, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $27, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-137438953473, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $4, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $26, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-274877906945, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $7, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $25, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-549755813889, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $6, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $24, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1099511627777, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $9, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $23, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2199023255553, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $8, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $22, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4398046511105, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $11, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2

```

```

; CHECK-NEXT: kshiftrq $21, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-8796093022209, %rax # imm = 0xFFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $10, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $20, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-17592186044417, %rax # imm = 0xFFFFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $13, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $19, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-35184372088833, %rax # imm = 0xFFFFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $12, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $18, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-70368744177665, %rax # imm = 0xFFFFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $15, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $17, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-140737488355329, %rax # imm = 0xFFFFF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $14, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $16, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-281474976710657, %rax # imm = 0xFFFFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $17, %k1, %k2
; CHECK-NEXT: kshiftlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $15, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-562949953421313, %rax # imm = 0xFFFFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $16, %k1, %k2

```

```

; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $14, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1125899906842625, %rax # imm = 0xFFFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $19, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $13, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2251799813685249, %rax # imm = 0xFFF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $18, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $12, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4503599627370497, %rax # imm = 0xFFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $21, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $11, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-9007199254740993, %rax # imm = 0xFFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $20, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $10, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-18014398509481985, %rax # imm = 0xFFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $23, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $9, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-36028797018963969, %rax # imm = 0xFF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $22, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $8, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-72057594037927937, %rax # imm = 0xFEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0

```

```

; CHECK-NEXT: kshiftrd $25, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $7, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-144115188075855873, %rax # imm = 0xFDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $24, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $6, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-288230376151711745, %rax # imm = 0xFBFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $27, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $5, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-576460752303423489, %rax # imm = 0xF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $26, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $4, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-1152921504606846977, %rax # imm = 0xEFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $29, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $3, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-2305843009213693953, %rax # imm = 0xDFFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $28, %k1, %k2
; CHECK-NEXT: kshiftrlq $63, %k2, %k2
; CHECK-NEXT: kshiftrq $2, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: movabsq $-4611686018427387905, %rax # imm = 0xBF7FFFFFFFFFFFFFFF
; CHECK-NEXT: kmovq %rax, %k2
; CHECK-NEXT: kandq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $31, %k1, %k2
; CHECK-NEXT: kshiftrlq $62, %k2, %k2
; CHECK-NEXT: korq %k2, %k0, %k0
; CHECK-NEXT: kshiftrd $30, %k1, %k1
; CHECK-NEXT: kshiftrlq $1, %k0, %k0
; CHECK-NEXT: kshiftrq $1, %k0, %k0

```

```

; CHECK-NEXT: kshiftrlq $63, %k1, %k1
; CHECK-NEXT: korq %k1, %k0, %k1
; CHECK-NEXT: vmovdqu8 %ymm1, (%rsi) {%k1}
; CHECK-NEXT: kshiftrq $32, %k1, %k1
; CHECK-NEXT: vmovdqu8 %ymm0, 32(%rsi) {%k1}
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
%a = load <64 x i8>, <64 x i8>* %x
%b = icmp eq <64 x i8> %a, zeroinitializer
%shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32
6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32
22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39,
i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32
55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, i32 1, <64 x i1> %shuf)
ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)

@mem64_dst = dso_local global i64 0, align 8
@mem64_src = dso_local global i64 0, align 8
define dso_local i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK: # %bb.0:
; CHECK-NEXT: kmovq mem64_src(%rip), %k0
; CHECK-NEXT: #APP
; CHECK-NEXT: #NO_APP
; CHECK-NEXT: kmovq %k0, mem64_dst(%rip)
; CHECK-NEXT: movl -{[0-9]+}(%rsp), %eax
; CHECK-NEXT: retq
%1 = alloca i32, align 4
%2 = load i64, i64* @mem64_src, align 8
%3 = call i64 @asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
store i64 %3, i64* @mem64_dst, align 8
%4 = load i32, i32* %1, align 4
ret i32 %4
}

define dso_local void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: cmp_v8i64_sext:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)

```

```

; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %yptr
%cmp = icmp slt <8 x i64> %x, %y
%ext = sext <8 x i1> %cmp to <8 x i64>
store <8 x i64> %ext, <8 x i64>* %zptr
ret void
}

```

```

define dso_local void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-vector-width"="256" {

```

```

; CHECK-LABEL: cmp_v8i64_zext:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT: vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT: vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT: vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT: vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
%x = load <8 x i64>, <8 x i64>* %xptr
%y = load <8 x i64>, <8 x i64>* %yptr
%cmp = icmp slt <8 x i64> %x, %y
%ext = zext <8 x i1> %cmp to <8 x i64>
store <8 x i64> %ext, <8 x i64>* %zptr
ret void
}

```

```

define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {

```

```

; CHECK-LABEL: var_rotate_v16i8:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa {{.*#+}} xmm2 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
; CHECK-NEXT: vpsubb %xmm1, %xmm2, %xmm2
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 =
xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zer
o,xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xm
m1[15],zero
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm0 =
xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zer
o,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xm
m0[15],zero
; CHECK-NEXT: vpsllvw %ymm1, %ymm0, %ymm1
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm2 =

```



```

; CHECK-AVX512-LABEL: constant_rotate_v32i8:
; CHECK-AVX512:    # %bb.0:
; CHECK-AVX512-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm2 =
ymm0[8],ymm1[8],ymm0[9],ymm1[9],ymm0[10],ymm1[10],ymm0[11],ymm1[11],ymm0[12],ymm1[12],ymm0[13
],ymm1[13],ymm0[14],ymm1[14],ymm0[15],ymm1[15],ymm0[24],ymm1[24],ymm0[25],ymm1[25],ymm0[26],ym
m1[26],ymm0[27],ymm1[27],ymm0[28],ymm1[28],ymm0[29],ymm1[29],ymm0[30],ymm1[30],ymm0[31],ymm1[
31]
; CHECK-AVX512-NEXT:  vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2
; CHECK-AVX512-NEXT:  vpsrlw $8, %ymm2, %ymm2
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm1 =
ymm0[0],ymm1[0],ymm0[1],ymm1[1],ymm0[2],ymm1[2],ymm0[3],ymm1[3],ymm0[4],ymm1[4],ymm0[5],ymm1[
5],ymm0[6],ymm1[6],ymm0[7],ymm1[7],ymm0[16],ymm1[16],ymm0[17],ymm1[17],ymm0[18],ymm1[18],ymm0[
19],ymm1[19],ymm0[20],ymm1[20],ymm0[21],ymm1[21],ymm0[22],ymm1[22],ymm0[23],ymm1[23]
; CHECK-AVX512-NEXT:  vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpsrlw $8, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpackuswb %ymm2, %ymm1, %ymm1
; CHECK-AVX512-NEXT:  vpunpckhbw {{.*#+}} ymm2 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:  vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2
; CHECK-AVX512-NEXT:  vmovdqa {{.*#+}} ymm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-AVX512-NEXT:  vpand %ymm3, %ymm2, %ymm2
; CHECK-AVX512-NEXT:  vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:  vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpand %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpackuswb %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  vpor %ymm1, %ymm0, %ymm0
; CHECK-AVX512-NEXT:  retq
;
; CHECK-VBMI-LABEL: constant_rotate_v32i8:
; CHECK-VBMI:    # %bb.0:
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm1 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT:  vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm1, %ymm1
; CHECK-VBMI-NEXT:  vpunpcklbw {{.*#+}} ymm2 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT:  vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2
; CHECK-VBMI-NEXT:  vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT:  vpermi2b %ymm1, %ymm2, %ymm3
; CHECK-VBMI-NEXT:  vpxor %xmm1, %xmm1, %xmm1
; CHECK-VBMI-NEXT:  vpunpckhbw {{.*#+}} ymm2 =
ymm0[8],ymm1[8],ymm0[9],ymm1[9],ymm0[10],ymm1[10],ymm0[11],ymm1[11],ymm0[12],ymm1[12],ymm0[13
],ymm1[13],ymm0[14],ymm1[14],ymm0[15],ymm1[15],ymm0[24],ymm1[24],ymm0[25],ymm1[25],ymm0[26],ym
m1[26],ymm0[27],ymm1[27],ymm0[28],ymm1[28],ymm0[29],ymm1[29],ymm0[30],ymm1[30],ymm0[31],ymm1[
31]

```


(an example is provided in the Appendix below).

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```
; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s
```

```
; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked  
; as Legal.
```

```
; Verify that fptosi(42.1) isn't simplified when the rounding mode is  
; unknown.  
; Verify that no gross errors happen.  
; CHECK-LABEL: @f20  
; COMMON: cfdetsiz  
define i32 @f20(double %a) strictfp {  
entry:  
  %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,  
    metadata !"fpexcept.strict")  
    strictfp  
  ret i32 %result  
}
```

```
@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)
```

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```
=====  
static_library("BSD-Archive") {  
  output_name = "lldbPluginObjectContainerBSDArchive"  
  configs += [ "//llvm/utils/gn/build:lldb_code" ]  
  deps = [  
    "//lldb/source/Core",  
    "//lldb/source/Host",  
    "//lldb/source/Symbol",  
    "//llvm/lib/Support",  
  ]  
  sources = [ "ObjectContainerBSDArchive.cpp" ]  
}
```

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1.15 httpparser 2.9.4

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1.16 sqlite 3.36.0

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1.18 zlib 1.2.7

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1.19 zlib 1.2.8

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/* zlib.h -- interface of the 'zlib' general purpose compression library
   version 1.2.11, January 15th, 2017
```

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*/
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1.20 curl 7.77.0

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1.21 json-c 1.2.11

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1.22 capnproto 0.7.0

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1.23 zlib 1.2.12

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* zlib.h -- interface of the 'zlib' general purpose compression library
version 1.2.12, March 11th, 2022

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1.24 sqlite 3.38.1

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1.26 bzip2 1.0.8

1.27 mbed-tls 2.6.0

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1.28 httpparser 2.7.1

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1.29 libevent 2.1.7-beta

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1.30 openssl 1.1.1k

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